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Defects inspection of the solder bumps using self reference technology in active thermography

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HIGHLIGHTS

- We proposed a method for reducing the impact of emissivity unevenness and heating non-uniformity.
- The method using the self reference technology is based on the source distribution image.
- Three thermograms captured right after heat pulse are averaged to create SDI.
- For the missing bump the summation of thermal difference is no more than 14 K.
- It is effective using the method to identify the defects in active infrared test.

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ABSTRACT

With the decrease of solder bumps in dimension and pitch, defects inspection of the solder bumps become more difficult. A nondestructive detection system based on the active thermography has been developed for solder bumps inspection. However, heating non-uniformities and emissivity differences may impede the defects recognition. In this paper, we propose a method using a self reference technology based on a source distribution image (SDI) to eliminate the influence of unevenness in emissivity values and heating power distribution. Three thermograms captured right after the heat pulse are averaged to create the SDI. Then the SDI is subtracted from the original thermograms, and we get the thermal contrast images, in which eight points on the edge of each hot spot are selected as the feature points for the corresponding bump. Thermal difference between the feature points and the central point are adopted to quantify the thermal behaviors of the solder bumps, by which the missing bump is distinguished from the reference bumps. The results show that it is effective using the method to eliminate the impacts of emissivity unevenness and heating non-uniformities on defects identification in the active infrared test.

1. Introduction

The miniaturization and multifunction desire of the IC devices have promoted the higher density in microelectronics packaging. The chip I/O pins are arranged in grid array instead of locating on the periphery. Surface mounting components, such as flip chips (FC), ball grid array (BGA) and chip scale packages (CSPs), using solder bumps to realize interconnection between chips/packages and substrates or printed circuit board (PCB), are extensively used in microelectronics packaging due to the decreased package size, greater I/O density and faster speed of signal propagation [1]. However, common manufacturing defects including open, cracked, or missing solder bumps are always existed. Since the solder bumps are hidden in the package after assembly, defects inspections become more and more difficult as the solder bumps develop towards high density and ultrafine pitch, which seriously hinders the development of surface mount technology. Defect inspection of the solder bumps becomes one of the key issues in IC manufacturing technology [2].

Current nondestructive testing methods for solder bump inspection can be divided into five categories [3]: (1) electrical testing, (2) optical visual testing, (3) X-ray inspection, (4) acoustic inspection, and (5) thermal inspection. These techniques are suitable only for specific defects inspection due to their disadvantages respectively. For electrical testing, it is effective for detecting the short and open circuit in chips, but it would pass the cracks and cold joints, which provide partial or intermittent electrical connections between chip and substrate. It is difficult to locate the solder defects and manufacturing the test pads also increases the cost. Optical visual testing is always used for inspecting visible solder joints or solder bumps before assembly. It becomes almost infeasible for the chip assembly as the hidden solder bumps deny the access of light beams [4]. X-ray inspection techniques [5,6]

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including radiography, laminography, and tomography, have been used for defects inspection of solder bumps. X-ray radiography applies the transmitted X-ray energy to indicate the inner situation of the package. It fails to detect fine cracks and open bump, because these defects with small air gap do not attenuate X-ray energy. X-ray laminography and tomography focusing the X-ray beam on one plane at a time and slicing the board horizontally, are effective 3D techniques which can detect almost all the defects in solder bumps. However the data acquisition and interpretation are time consuming and the equipment and operation cost are unaffordable. Acoustic techniques are effective for inspection of voids and interfacial delaminations in electronic packages, while the main drawbacks are poor resolution caused by sound scattering at object edges and the requirement for a coupling medium [7,8]. Thermal imaging inspection operates on the premise that defects exhibit different thermal behaviors from the reference, which provides a fast, non-contact and full field measurement. But surface conditions and emissivity differences may influence the resolution and infrared image contrast adversely [9].

Other inspection methods have also been investigated. Liu and Ume developed a nondestructive system using laser ultrasound and interferometer techniques to measure the transient out-of-plane displacement response of the electronic package under pulsed laser excitation [10,11]. It is effective to detect the solder bumps with large diameter and pitch. Chai utilized the hot spots in thermal images to identify the defective solder bumps when the electrical current passing through the daisy chained chips [12,13]. Defects such as a partial solder joint crack with an increased electrical resistance are identified.

In our previous work, a non-destructive detection system based on the active thermography has been developed to inspect defects of the solder bump [14], in which the test chip is excited by a thermal pulse and the consequent transient response is monitored by an infrared thermal imager. The defects are distinguished by the abnormal thermal behavior. However, the heating source plays a significant role on the infrared testing. Heating non-uniformities may impede the defects recognition. In this paper, we propose a method to eliminate the effects of emissivity unevenness and heating non-uniformities on defects identification. The heating source distribution image has been constructed and the self reference technology is adopted to quantify the thermal behaviors of the solder bumps.

2. Experiment description

The inspection system using active thermography has been developed, in which a commercial thermal imager of VH 680 is used to measure the transient response of the test chip under the thermal excitation of the heating source. Temperature resolution of the thermal imager is better than 80 mK, and the frame size is 640 × 480 pixels. A microscopic lens with the pixel resolution of 25 μm is equipped for the thermal imager to improve the spatial resolution. The fiber-coupled semiconductor laser with the center wavelength of 808 nm is used as the heating source. The optical image of the test vehicle SFA2 before assembly is shown in Fig. 1. There are 16 solder bumps arranged in an array of 4 × 4 pattern, one of which in up-left corner has been removed deliberately in order to introduce the defect of missing bump when the chip is bonded to the substrate. The solder bumps are 300 μm in diameter and spaced with a pitch of 600 μm. The thickness of the silicon substrate is about 300 μm.

The experimental setup was deployed as depicted in Fig. 1, where the samples were inspected in transmission way during the test procedure. The silicon substrate is excited by a laser pulse heating, which is 200 ms in duration and the maximum pulse energy is 240 mJ. Temperature evolutions of the die surface are monitored by the thermal imager and then are processed to identify the defects in the package.

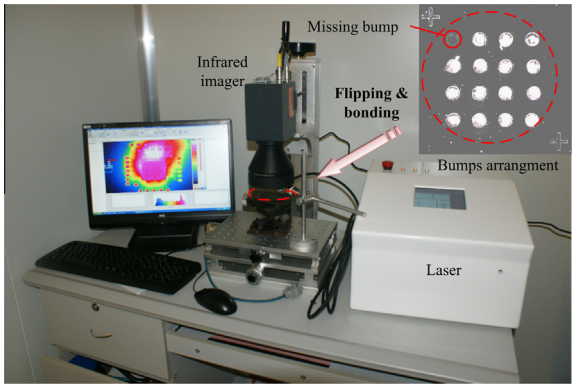

Fig. 1. Experimental deployment and solder bumps arrangement of the SFA2.

3. Theory analysis and methodology

3.1. Heat conduction analysis

Fig. 2 illustrates the structure with single layered chip and substrate, in which the silicon die is attached to the substrate by a solder bumps array. When a thermal excitation is activated, the heat exchange would occur in the package [15]. As known, heat transfer in the solid body is governed by the Fourier diffusion equation, which describes the distribution and variation of temperature in a given region and time,

$$\frac{\partial T}{\partial t} = \frac{k}{\rho c_p}\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{Q}{\rho c_p} \tag{1}$$

where $T = T(x,y,z,t)$ depicts the temperature at the point (x,y,z) and time t, k denotes the thermal conductivity, ρ is the density and c_p the specific heat capacity, and Q is defined as the internal heat generation per unit volume in unit of W/m^3.

There are no internal heat sources in the package because the chip is not in working condition [16]. We will put emphasis on the investigation of the heat conduction via solder bumps and the estimation of defects influence on thermal behavior in the active infrared inspection.

In the transmission way, a heating pulse is imposed on the bottom surface of the substrate, and the thermal front is launched and propagates inside the structure. As the thermal front reaches the top surface of the substrate, it would propagate into the chip via solder bumps, or be hampered by the defects and then flow to adjacent solder bumps, as depicted in Fig. 2. When observed from

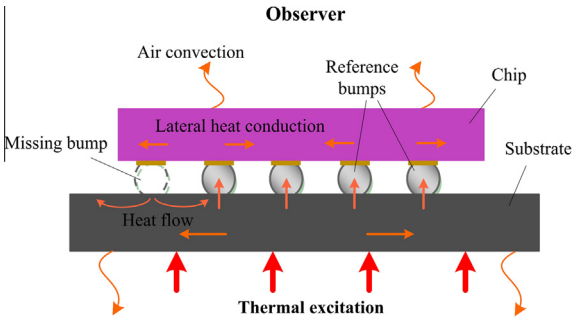

Fig. 2. Schematic of heat conduction via solder bumps.