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Embedded nonuniformity correction in infrared focal plane arrays using the Constant Range algorithm

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HIGHLIGHTS

- We present a digital hardware architecture for real-time NUC in IR embedded imagers.
- We designed and implemented a prototype in a field-programmable gate array (FPGA).
- We designed and simulated a custom integrated circuit version of the architecture.
- We present experimental results from the FPGA prototype.

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ABSTRACT

We present a digital fixed-point architecture that performs real-time nonuniformity correction in infrared (IR) focal plane arrays using the Constant Range algorithm. The circuit estimates and compensates online the gains and offsets of a first-order nonuniformity model using pixel statistics from the video stream. We demonstrate our architecture with a prototype built on a Xilinx Spartan-6 XC6SLX45T field-programmable gate array (FPGA), which can process an IR video stream from a FLIR Tau 2 long-wave IR camera with a resolution of 640 × 480 14-bit pixels at up to 238 frames per second (fps) with low resource utilization and adds only 13 mW to the FPGA power. Post-layout simulations of a custom integrated circuit implementation of the architecture on a 32 nm CMOS process show that the circuit can operate at up to 900 fps at the same resolution, and consume less than 4.5 mW.

1. Introduction

Thermal vision systems relying on infrared (IR) cameras are extensively used in a diverse set of application areas, which include surveillance and security, medical imaging, fire rescue operations, and health care, among others. Due to operational conditions and technology limitations in the fabrication of the detectors in the Infrared Focal Plane Array (IRFPA) and the readout circuitry, the response of the IR camera, when stimulated with a uniform radiation source, is not homogeneous [1,2]. This nonuniformity (NU) in the response of the IRFPA manifests itself as a fixed-pattern noise in the output image [1,2].

The severity of the effects of this nonuniform response varies depending on the technology of the IRFPA, calling for nonuniformity correction (NUC) techniques to generate an adequate output for most applications [1,2]. Even when the effect is not visually intrusive, the presence of fixed-pattern noise on the images degrades the performance of various image processing algorithms that can be used in later stages of the visualization system, such as digital image stabilization, super resolution, and image registration [1,2]. Moreover, because the exact parameters of the fixed-pattern noise depend on the initial conditions of the IRFPA and drift over time, it is impossible to perform a one-time factory calibration of the device [1,3,4].

NUC algorithms are particularly attractive for implementations on embedded and portable IR visualization systems that integrate video processing capabilities in the camera, such as hand-held or mounted devices. The ability to correct images in real time at the native frame-rate and resolution of the imager are appealing camera features. Because typical NUC algorithms are computationally expensive, the embedded hardware executing the algorithm must provide high performance while operating under severe restrictions in power, size, and cost. In many applications, common programmable devices such as microprocessors and digital signal processors (DSPs) cannot deliver the performance needed by the application under these restrictions, especially if the device must

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also perform higher-level video processing tasks such as super resolution [5,6], video stabilization [7,8], face detection [9,10]. In these cases, dedicated hardware solutions may be needed in order to achieve the performance/power/size/cost tradeoff required by the application.

In this work, we present a digital hardware architecture for the Constant Range (CR) scene-based NUC algorithm [11,12] implemented on a custom integrated circuit and a field-programmable gate array (FPGA), which provide higher performance, data bandwidth, and power efficiency than traditional programmable solutions such as embedded computers or DSPs. The architecture can acquire a video stream from the digital output of the readout circuitry of the camera, or process a video stream over a high-speed network interface. The architecture exploits the data parallelism and limited spatial and temporal dependencies available in the algorithm to achieve good computational performance with low power. We implemented a prototype of our architecture on a Xilinx Spartan-6 FPGA, which reads an IR video stream from the CMOS LVDS output of a FLIR Tau 2 LWIR camera core and displays the NU-corrected video on an external monitor using an HDMI interface. The prototype can also receive raw video and send the corrected output over a local network using a Gigabit Ethernet interface. The same interface can be used to configure the device and modify local parameters. We also designed an Application-Specific Integrated Circuit (ASIC) implementation of the architecture on 0.5 μm and 32 nm CMOS very-large scale integration (VLSI) processes, which can achieve even better performance and lower power.

The rest of the paper is organized as follows. Section 2 describes the body of work on NUC algorithms and dedicated hardware implementations of such algorithms. Section 3 describes the CR algorithm used in our solution. Section 4 describes the proposed architecture in detail. Section 5 discusses the system-level implementation of our FPGA prototype, and describes the custom ASIC design. Section 6 shows implementation details and experimental results. Finally, Section 7 concludes the paper and outlines our future work.

2. Related work

The techniques used to perform NUC in IRFPAs can be broadly divided into two categories: reference-based and scene-based methods. Reference-based NUC methods calibrate the response of the IR camera using external temperature references such as black-body radiators. The most common reference-based NUC method is the two-point calibration (TPC) procedure [13], which measures the response of the camera at two different spatially uniform temperatures to compute the NUC parameters. Reference-based methods use temperature references, allowing the radiometric calibration of the camera. Due to the temporal drift of the NU parameters, it is necessary to periodically recalibrate the IR camera by interrupting its normal operation. This can be impractical in real-time or mission-critical applications. Moreover, black-body radiators are large and expensive, presenting additional limitations for on-site calibration.

Scene-based NUC methods rely on assumptions on the statistics of the video stream to perform correction without an external reference. These techniques continuously correct the video stream without interrupting the normal operation of the IR camera, and do not require large and/or expensive reference sources such as black-body radiators. Unlike reference-based methods, they naturally track variations in the NU parameters. The underlying assumptions on the statistics of the video require the presence of motion in the scene; otherwise, the NUC algorithm may produce undesired ghosting artifacts [14]. To reduce ghosting, some methods use adaptive learning-rate strategies, or allow correction only in the presence of motion [15,16]. In spite of their intrinsic limitations, the practical advantages offered by scene-based algorithms make them attractive solutions for mobile and embedded IR imaging, specially when radiometric accuracy is not needed. Therefore, the rest of this work focuses on this class of algorithms.

Scribner et al. proposed a neural network that emulates the operation of the human retina [3]. The neural network adapts the NU correction parameters using the steepest descent, linear regression algorithm with a local spatial averaging of the nearest neighbors as the desired outputs. Harris and Chiang developed the constant statistics algorithm [4], which assumes that the mean and variance of the incident radiation seen by every detector in the IRFPA follows a Gaussian distribution, with zero mean and unitary standard deviation. Thus, the mean and variance of the detectors are compensated in order to obtain such statistical distribution on the outputs. Unlike Harris and Chiang, Hayat et al. [17] introduced the concept of CR by proposing that the global statistics for the incident radiation on an IRFPA has a uniform distribution. Using this supposition, they devised a discrete-time Wiener filter to compensate the NU gain and offset. Later, the CR algorithm was proposed by Torres [11,12]. This method compensates the NU in IR video sequences assuming that the global statistics of the input IR irradiance follows an uniform distribution in a known radiation range. Also under the CR assumption, and considering the gain and offset of the detectors as state variables modeled by a Gauss-Markov random process, Torres developed a Kalman filter to estimate the NU parameters [18]. San Martin simplified the previous Kalman filter by assuming that the temporal drift of the gain is practically negligible [19], and only estimated and compensated for the NU offset. Geng et al. presented a method based on an improvement of the constant statistics method [20], where a temporal median filter combined with a Gaussian kernel were used to estimate NUC parameters by taking the advantage of the median filter robustness to variation on the sample distributions. Other methods rely on motion constraints, like the one proposed by Zuo et al. [21], which estimates motion between two adjacent frames using a phase-correlation method. The gain and offset NU were calculated to minimize the mean squared error between both aligned images.

To achieve the constraints for real-time video, some works integrate NUC algorithms with the sensing technology, using architectures based on FPGAs in cooperation with external or embedded processor. Most works program the high-level or sequential work in the processor, while the logic of the FPGA is used as a hardware accelerator. Following this scheme, Sosnowski developed a dedicated hardware that implements two-point calibration for NUC [22]. This platform used a Philips LPC2292 microprocessor for array control and temperature measurement, and an Altera Quartus-II FPGA for NUC and video display. The system processed video frames of 284×288 14-bit pixels on line, and could achieve a maximum frequency of 68.1 MHz, more than ten times the 6.25 MHz required by the design. Zou also implemented a reference-based NUC using a pipelined architecture on an Altera NIOS II FPGA, and used an external DSP for image processing and pattern recognition [23]. This system also used the embedded processors on the FPGA to update NUC parameters during calibration, and to control data and external memory transactions. The complete architecture can process up to 100 fps on frames of 320×240 pixels using around 38% of the logic resources of the FPGA, and consumes 832 mW. Toczek developed a hardware implementation of an improved version of the constant statistics algorithm [24]. This method compensated the offset by removing the spatial low frequencies of each frame before applying the constant statistics technique, and then added the low frequencies to the final image. The algorithm produced corrected images with a peak signal-to-noise