Infrared Physics & Technology 53 (2010) 254–266

Contents lists available at ScienceDirect

Infrared Physics & Technology

journal homepage: www.elsevier.com/locate/infrared

A pipelined architecture for real time correction of non-uniformity in infrared focal plane arrays imaging system using multiprocessors ☆

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ARTICLE INFO

Article history:
Received 11 August 2009
Available online 27 March 2010

Keywords:
HW/SW co-design
Multiprocessor
Non-uniformity correction
Pipelined
Real time
SOPC

ABSTRACT

This paper proposes a kind of pipelined electric circuit architecture implemented in FPGA, a very large scale integrated circuit (VLSI), which efficiently deals with the real time non-uniformity correction (NUC) algorithm for infrared focal plane arrays (IRFPA). Dual Nios II soft-core processors and a DSP with a 64+ core together constitute this image system. Each processor undertakes own systematic task, coordinating its work with each other's. The system on programmable chip (SOPC) in FPGA works steadily under the global clock frequency of 96Mhz. Adequate time allowance makes FPGA perform NUC image pre-processing algorithm with ease, which has offered favorable guarantee for the work of post image processing in DSP. And at the meantime, this paper presents a hardware (HW) and software (SW) co-design in FPGA. Thus, this systematic architecture yields an image processing system with multiprocessor, and a smart solution to the satisfaction with the performance of the system.

1. Introduction

Making a Comparison with other thermal imaging systems, infrared focal plane arrays (IRFPA) imaging system has its excellence, e.g., its high packing density, low cost, reduced signal leads through the dewar, high feasibility on chip signal processing, and high flexibility for system integration and so on [1–3]. It has wide application prospect in infrared imaging fields [4], such as astronavigation, military, robotics. But the equipment of infrared focal plane array (IRFPA) also has its inner defect. For example, the non-uniformity of its response is its important technical problem in application that must be solved [1,5,6].

The non-uniformity of infrared focal plane array image becomes the fixed-pattern noise (FPN) on the images, which worsen seriously the temperature resolution of infrared image [1]. So, nearly all infrared focal plane arrays equipments will apply non-uniformity correction techniques.

In view of that researchers have made plenty of work on the non-uniformity correction (NUC) algorithm for infrared focal plane arrays, and have gained satisfactory accomplishments [7–27]. But, hitherto, in this field, there have not been enough research about the topic on "How do we apply multiprocessor technique, a powerful and arrogant computer technology field at present, to improve the systematic performance, when we come across a rigid requirement of systematic real time." So, this article does not emphasize the research of this algorithm itself and its related theory, but, only for its realization method, makes the detailed research and discussion. Now, some comparison and analysis are made between some predecessors' methods and ours.

Up to now, the realization method for real-time NUC algorithm of on chip digital signal processing in practical implementation has mainly divided into four catalogs:

1. Based on the software in DSP [28].
2. Based on the architecture of DSP and FPGA [29].
3. Based on the mere customized hardware module in FPGA of high performance [30–32].
4. And based on the customized hardware module plus single embedded soft-core microprocessor in FPGA [33].

Thus, we develop a discussion among all on chip digital signal processing methods. To DSP based means [28], they will not be put into consideration because, in our system, DSP plays a more significant role to perform some more sophisticated algorithms, that is, so-called post image processing. So, in the period of preprocessing of image, to reduce its burden is essential in order to gain a high performance in term of the entire image processing system. As far as FPGA based methods are concerned [30–33], they are almost cannot exert all the potential of hardware efficiency to improve systematic throughput. To the method based on

☆ This work is sponsored by the NSFC, PR China, under Grant No. 60875058, and the national 863 Program under Grant No. 2007AA04160X, and RFDP (The Research Fund for the Doctoral Program of Higher Education), under Grant No. 20070248021, and 2008 SMC Excellent Youth Teacher Award of SJTU.

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doi:10.1016/j.infrared.2010.03.001

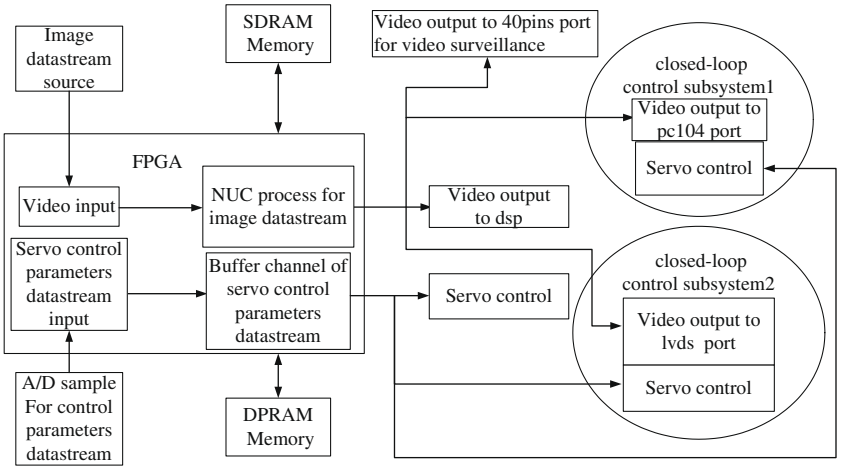

Fig. 1. A conceptual schematic of hardware architecture.

DSP&FPGA [29], it belongs to a conventional method to realize NUC algorithm in FPGA.

In this paper, we present a novel realization method of HW/SW co-design with hardware pipeline technique, and multiprocessor technique. Pipelining is the method to partition the workload of any task into equal subtask is greatly reduced compared to the time to complete the whole task. Therefore, the system can run with much higher clock frequency [34]. And using these techniques, we have successfully realized high speed and real time non-uniformity correction algorithm and complicated multi-channels dataflow communication tasks. Our system schematic diagram is shown in Fig. 1, which, in the rough, shows the heavy communication tasks, which the real-time image system must accomplish.

2. A HW/SW co-design for the realization of real-time NUC algorithm based on hardware pipeline technique and multiprocessor architecture

2.1. An overview of reference-based NUC algorithm for infrared focal plane arrays realized in FPGA

NUC techniques can divide into two types [10]. One relies on the known blackbody calibration-source, such as two-point or multi-point calibration techniques, that is, reference-based NUC algorithm. The other is focused on some scene-based algorithms. And each has its advantage. To reference-based NUC algorithms, such as, two-point calibration (TPC) technique corrects both gain and offset variations, in theory it can completely correct the detectors non-uniformity although it is not very precise under the circumstance when the dynamic range of detector is large. However, its low calculation complexity results in its ability to be real-time realized in hardware [18]. To put this fact into account, we adopt this algorithm in the article. And TPC contemporarily satisfies our application in principle prototype.

What is TPC? According to the radiation range of scene that IRFPA observes, two irradiances are chosen as the correction points, and the detector response data under the two points are recorded respectively. In this paper we utilize twin images under different temperature to represent the twin irradiances, e.g. a frame of image from a high temperature and a respective low one, derived from infrared focal plane array (IRFPA) image equipment. The definition of frame is $M \times N = 320 \times 256$ pixels. Every pixel is expressed by the format of 16 binary numbers. Two frames of image may be expressed by matrices $X_{M\times N} = X_{320\times 256} = \begin{bmatrix} x_{1,1} & \cdots & x_{1256} \\ \cdots & \cdots & \cdots \\ x_{320,1} & \cdots & x_{320,256} \end{bmatrix}_{320\times 256}$ and $Y_{M\times N} = Y_{320\times 256} = \begin{bmatrix} y_{1,1} & \cdots & y_{1256} \\ \cdots & \cdots & \cdots \\ y_{320,1} & \cdots & y_{320,256} \end{bmatrix}_{320\times 256}$, respectively. Their respective elements are x_{ij} and y_{ij}.

Where (i, j) are the coordinates of a detector in the array.

The average values of matrix elements are calculated from the twin original image matrices:

$$\overline{X}_{M\times N} = \frac{1}{M\times N}\sum_{i=1}^{M}\sum_{j=1}^{N} x_{ij} \tag{1}$$

$$\overline{Y}_{M\times N} = \frac{1}{M\times N}\sum_{i=1}^{M}\sum_{j=1}^{N} y_{ij} \tag{2}$$

And, the correction parameter matrices $A_{M\times N} = A_{320\times 256} = \begin{bmatrix} a_{1,1} & a_{1,2} & \cdots & a_{1256} \\ a_{2,1} & a_{2,2} & \cdots & a_{2256} \\ \cdots & \cdots & \cdots & \cdots \\ a_{320,1} & a_{320,2} & \cdots & a_{320,256} \end{bmatrix}_{320\times 256}$ and $B_{M\times N} = B_{320\times 256} = \begin{bmatrix} b_{1,1} & b_{1,2} & \cdots & b_{1256} \\ b_{2,1} & b_{2,2} & \cdots & b_{2256} \\ \cdots & \cdots & \cdots & \cdots \\ b_{320,1} & b_{320,2} & \cdots & b_{320,256} \end{bmatrix}_{320\times 256}$, whose respective elements are a_{ij} and b_{ij}, are obtained, according to the following formulae:

$$\overline{X}_{M\times N} = \frac{1}{M\times N}\sum_{i=1}^{M}\sum_{j=1}^{N} x_{ij} = a_{ij}x_{ij} + b_{ij} \tag{3}$$

$$\overline{Y}_{M\times N} = \frac{1}{M\times N}\sum_{i=1}^{M}\sum_{j=1}^{N} y_{ij} = a_{ij}y_{ij} + b_{ij} \tag{4}$$

Thus

$$a_{ij} = \frac{\overline{x}_{ij} - \overline{y}_{ij}}{x_{ij} - y_{ij}} \quad i = 1, 2, \ldots, M,\ j = 1, 2, \ldots, N \tag{5}$$

$$b_{ij} = \overline{x}_{ij} - \frac{\overline{x}_{ij} - \overline{y}_{ij}}{x_{ij} - y_{ij}} \times x_{ij} \quad i = 1, 2, \ldots, M,\ j = 1, 2, \ldots, N \tag{6}$$

The algorithm that needs realizing in FPGA is formula (7) shown below:

$$U_{ij} = a_{ij} \times V_{ij} + b_{ij} = \frac{\overline{x}_{ij} - \overline{y}_{ij}}{x_{ij} - y_{ij}} \times V_{ij} + \left(\overline{x}_{ij} - \frac{\overline{x}_{ij} - \overline{y}_{ij}}{x_{ij} - y_{ij}} \times x_{ij}\right) \tag{7}$$