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Investigation of rapid thermal oxide/ silicon nitride passivation stack of n^+ emitter

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ABSTRACT

To anticipate the initial phosphorus diffusion parameters of silicon solar cells process fabrication, we report in this paper an overview of our experiments on silicon n^+-emitters passivation by means of rapid thermal silicon oxide/silicon nitride stack. The process-induced changes have been evaluated and explained. We found that 900 °C and 80 s were the appropriate process parameters to grow 10 nm silicon oxide. Investigation of the effect of this oxidation on n^+ multicrystalline silicon emitters revealed a large decrease (more than 25%) of the sheet resistance and around 12% increase of the junction depth. The experiments also revealed that the passivation effect of the optimal silicon oxide/silicon nitride stack is efficient only for higher emitter quality. In addition, we found that this stack reduces the surface reflection more than the optimal single silicon nitride layer.

1. Introduction

Increasing the conversion efficiency of crystalline silicon solar cells is the most important objective of silicon photovoltaic research. Highly efficient solar cells are obtained only when both the loss of sunlight entering into solar cells and the loss of photo-generated carriers are low [1]. In order to further reduce these losses, various studies and methods have been investigated these last years. For front side p-type monocrystalline silicon solar cells, these studies included surface texturing, antireflection coating (ARC), gettering and surface passivation by hydrogenation.

Besides the silicon nitride (SiN) film which acts as ARC and passivating layer, the silicon oxide (SiO_2) is also a material which has been extensively studied and used thanks to its established passivation and ARC properties. Using a classical thermal SiO_2 (CTO) by means of a conventional tube furnace, a very high passivation quality can be achieved even though the wafer is processed at very high temperatures [2]. Because of its low thermal budget, the rapid thermal oxidation (RTO) is an interesting method to grow a SiO_2. In comparison to the CTO, the RTO reduces the oxidation time by a factor of more than 20. In addition, the qualities of these two passivation techniques are comparable [3]. Another advantage of the RTO passivation is that there is no difference in the chemical structure between RTO and CTO SiO_2 [4].

The drawback of the SiO_2 used as ARC is its thickness. A 100 nm thick is required whereas the combination of a very thin layer of SiO_2 and plasma enhanced chemical vapour deposition (PECVD) SiN film appears as a promising candidate [5–7]. A SiN layer deposited onto thin SiO_2 constitutes an efficient stack for emitter surface passivation [8–10]. The SiO_2 is used for its thermal stability, low interface defect density [11] and to maintain the desired device electrical properties [12]. In addition, the RTO/SiN stack presents the advantage that both RTO and SiN are not only fast but also low-cost processes.

At present, the same SiO_2/SiN stack is widely used in n-type monocrystalline silicon solar cells industry [13,14]. This is because of the standard passivation layer SiN [15,16] as well as thermally grown SiO_2 layers [15,17] has shown a poor performance on p^+-emitter. Moreover, according to the International Technology Roadmap for Photovoltaic (ITRPV) report [18] which predicts a shift from p-type to n-type within the monocrystalline silicon material market, we expect a greater use of the SiO_2/SiN stack in the photovoltaic industry.

We present in this paper an overview of our experiments on silicon n^+-emitters passivation using a RTO/PECVD SiN stack and its process-induced changes. We will focus on the changes of physical and electrical parameters of n^+ emitters subjected successively to RTO and SiN deposition process. Evaluation of these changes may serve for anticipating the initial phosphorus diffusion and metallization parameters of solar cells process.

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2. Experimental

The study of the SiO_2 growth was achieved on 4-inch mirror-polished (m-p) RCA cleaned <100> p-type monocrystalline CZ wafers. A single wafer rapid thermal process furnace from Allwin (Accu Thermo AW610) was used. The SiO_2 thickness was measured by means of an ELX 02C (DRE Gmbh) ellipsometer operating at 632.8 nm.

Investigation of the passivation effect of RTO/SiN stack was performed using neighboring 4-inch HEM p-type multicrystalline (mc-pSi) 1–2 Ω cm silicon wafers. Fig. 1 shows the sequential process steps used for achieving the device structure. The n^+ emitters were performed using $POCl_3$ quartz tube furnace. SiN films were deposited in a direct-plasma pulsed reactor operating at low frequency using a mixture of pure silane (SiH_4) and pure ammonia (NH_3).

The n^+ emitter sheet resistance (Rsh) was measured by means of a four-point probes technique. The passivation quality was assessed using the quasi-steady-state photoconductance (QSSPC) technique. A Sinton WCT 120 station was used to measure the minority carrier lifetime on symmetrically processed wafers-test.

3. Results and discussion

3.1. Study of the SiO_2 growth on silicon substrate

Preliminary experiments were conducted in order to determine the RTO parameters which lead to about 10 nm SiO_2 thickness. To avoid possible carrier lifetime deterioration, a reduced process time and low temperature were preferred. The typical RTO profile used is shown in Fig. 2.

3.1.1. Determination of the minimum process temperature

In this section we kept constant the oxygen at its maximum flow rate of 10 standard liters per minute (slpm) and the plateau time at 80 s. Three plateau temperatures (T°max) were used: 850 °C, 950 °C and 1000 °C.

As shown in Fig. 3, the SiO_2 grows linearly with T°max. The thickness varies from 5 nm to around 20 nm when the temperature increases from 850 °C to 1000 °C. Fig. 3 also indicates that the lowest plateau temperature to reach about 10 nm SiO_2 thickness is 900 °C. Temperature below 900 °C requires out of range oxygen flow rate. Furthermore, taking into account that the maximum duration of T°max is 5 min (furnace technical limitation), we deduced that the maximum SiO_2 thickness which can be reached with this RTO furnace is 37 nm at the temperature of 900 °C.

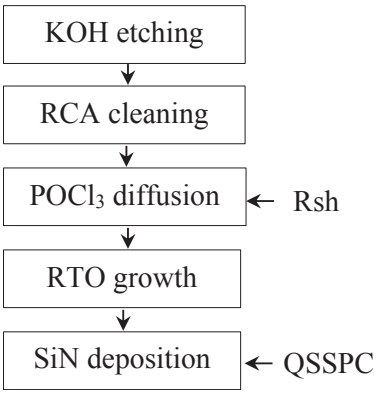

Fig. 1. Flow chart of the sequential steps and corresponding characterization.

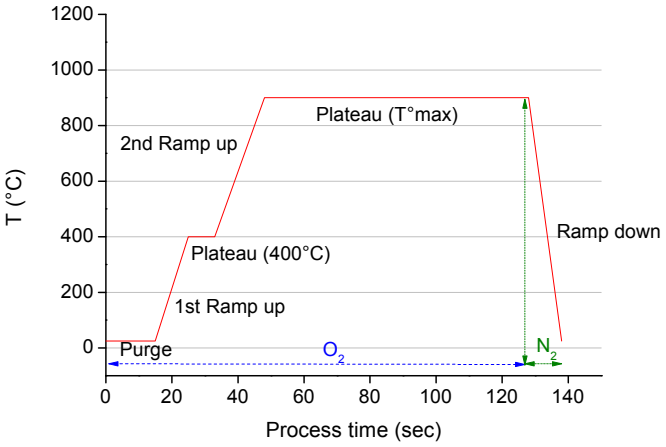

Fig. 2. Typical RTO profile used.

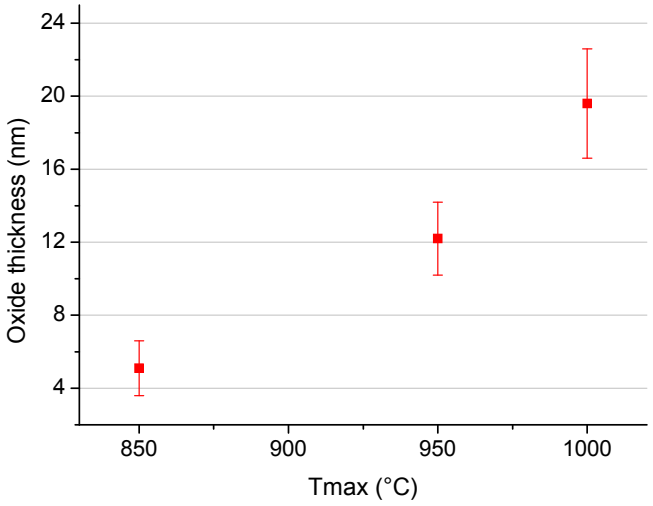

Fig. 3. SiO_2 thickness as a function of T°max (Plateau time of 80 s and 10 slpm O_2).

3.1.2. Determination of oxygen flow rate

Fig. 4 shows the SiO_2 thickness for 9 slpm and 10 slpm oxygen flow rates in dependence of the plateau time. The SiO_2 growth rate

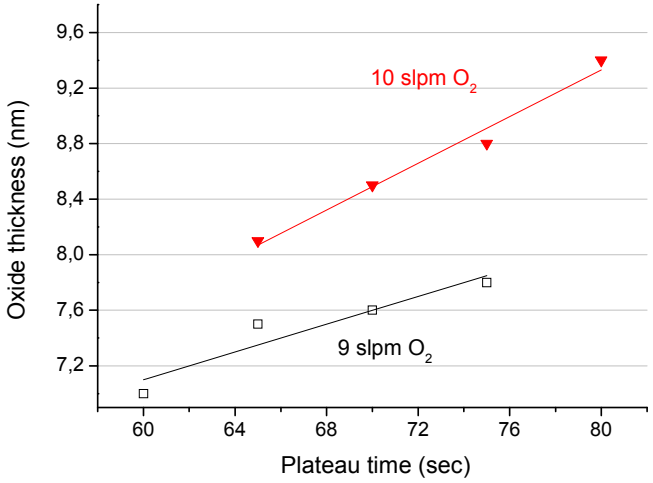

Fig. 4. SiO_2 growth rates at Tmax = 900 °C for 9 slpm and 10 slpm oxygen.