



Evolution of various quantum transport properties in a suspended disordered graphene device by the high bias voltage exposure



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ABSTRACT

We investigated the evolution of the electronic transport properties of a suspended disordered graphene device by systematically controlling the bias voltage. Previously, the application of high bias voltage resulted in the sudden constriction of a graphene device. During the high bias voltage process, we utilized an electronic feedback loop to prevent the sudden change in resistance to ensure that the constriction proceeded sufficiently slowly. We performed a total of 137 sequential steps of a controlled high bias voltage exposure on the device in a cryostat. After each exposure, we measured the electronic transport properties and observed the transformation between various intriguing quantum transport phenomena. When the overall conductance was suppressed below approximately 10% of the single quantum conductance, superimposed Coulomb diamond patterns appeared at low temperatures, exhibiting parallel double quantum dot behaviors. We also found that the parallel double quantum dots were transformed into a single quantum dot and then into a single tunnel barrier as the high-voltage exposure was applied repeatedly. The transformation of the electronic transport properties along with the high bias voltage exposure processes can be attributed to the gradual reduction of the graphene width.

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1. Introduction

Lithographically patterned graphene nanostructures show various intriguing quantum transport properties [1]. In particular, reducing the graphene width to form a graphene nanoribbon (GNR) has gained attention because the quantum confinement energy gap (ΔE_{con}) has the potential to lead to more practical applications than gapless graphene [2]. The confinement gap, where the conductance is strongly suppressed, is inversely proportional to the graphene width ($E_g \sim 1/W$). Accordingly, a very narrow GNR exhibits high on-off switching capabilities. The appearance of a quantum dot was reported in the presence of a confinement gap accompanied by a strong bulk and edge-induced disorder potential (Δ_{dis}) [3,4]. Various quantum transport properties were attributed to device-specific properties that were determined by the confinement gap and disorder potentials [5,6].

In the case of lithographically patterned graphene nanostructures, it is difficult to construct a device with an ultra-narrow

width. Moser et al. [7] presented an interesting technique to fabricate a small-sized quantum dot device. By applying a large current through a suspended graphene device and then reducing the current back to zero within 10 ms, after the conductance fell to a low value, they found clear Coulomb diamond patterns in some devices. The formation of a quantum dot was ascribed to the appearance of an ultra-narrow constriction combined with potential fluctuation along the constriction. The authors confirmed the ultra-narrow constriction with a scanning electron microscope (SEM) image, and the size of the quantum dot was approximately 20 nm. Some devices exhibited single electron transistor (SET) behavior, whereas other devices showed the signatures of a series of SETs. One of the devices exhibited a particularly large I(V) gap, which was not clearly understood. Different electronic transport properties for other devices can be related to the momentary constriction caused by a sudden rupture.

Recently, a number of studies related to nanoconstriction were reported [7–12]. Prins et al. [8] used a feedback-controlled electroburning method. Different from the previous sudden constriction method, this constriction process was carefully modulated by detecting the variations in the conductance with a feedback

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process. Most of the devices showed a large transport $I(V)$ gap with low bias resistance in the range of 0.5–10 G Ω . An atomic force microscope (AFM) study confirmed the presence of a nanogap. Candini et al. [9] fabricated large $I(V)$ gap devices using the feedback control of electronics that restored the bias voltage to zero very rapidly (<100 μ s). The SEM image of these devices showed a similar nanogap that was adjacent to the high-voltage-induced constriction. The authors explained that the nanogap was a tunnel barrier and induced a large transport gap in the IV characteristics. Barreiro et al. [10] presented an in situ TEM investigation that showed the real-time evolution of a constriction. The bias voltage applied to the suspended CVD graphene was increased very carefully until the current flowing through the device decreased as a function of time. By keeping the bias voltage constant, the authors found the formation of a crack on one edge that propagated toward the other edge of the sample. The appearance of a nanoconstriction can be attributed to the high bias voltage exposure processes.

In the present study, we achieved the progressive transformation of the various states of a quantum transport in a single nanoconstricted graphene device. We first fabricated a suspended graphene device and performed the high bias voltage exposure process at low temperature in a cryostat. We increased the bias voltage in a very meticulous manner so that the formation of the nanoconstriction was properly controlled. During the process, we maintained a gradual change in the resistance, and the width of the nanoconstricted graphene devices could be reduced gradually. We observed that the quantum transport properties of nanoconstricted graphene devices varied as the width of graphene devices was decreased.

2. Methods

2.1. Fabrication

Suspended graphene devices were fabricated with the method proposed by Tombros et al. [13] A total of 150 nm of LOR-a (Microchem) was spin coated onto a p -doped silicon wafer that had been coated with 300 nm of oxide. Subsequently, one or two layers of graphene were deposited by the standard “scotch tape” mechanical exfoliation method from natural graphite pieces onto the LOR-coated silicon wafer. Individual narrow graphene flakes were located by thoroughly examining the surface of the wafer with an atomic force microscope. The electrode patterns were obtained in the first step of the e-beam lithography process. Next, 25 nm Pd electrodes were deposited by an e-beam evaporator. To suspend the graphene devices, the LOR underneath the graphene devices was selectively developed in the second step of the e-beam lithography. The suspended graphene device was then supported by solid pillars of LOR. A schematic diagram of the fabricated device is shown in Fig. 1a.

2.2. High bias voltage exposure

Fig. 1b shows the controlled high bias voltage exposure process (detailed procedure is described in Supplementary Information). The bias voltage was increased by 10 mV steps every 3 s in low temperature (1 K) cryostat. Initially, when the bias voltage was increased by a step of 10 mV, the resistance jumped to a certain value and did not change as a function of time. We continued to increase the bias voltage until the resistance did change as a function of time after the step change of the bias voltage. Thereafter, we either increased or decreased the bias voltage to ensure that the variation phase proceeded at a sufficiently slow rate. The resistance change rate, dR/dt , is strictly controlled with a positive and/or negative feedback loop. When a rapid change in the

resistance could not be stalled quickly, the bias voltage was reduced to zero by a very slow reduction rate (10 mV in 3 s). The high voltage exposure time for each process varied widely from 30 to 300 min.

After each process, the electronic transport properties were obtained by conductance (I/V) and differential conductance (dI/dV) measurements. Both were measured as a function of a back gate voltage at 1 K. A two-dimensional differential conductance map, as functions of bias and gate voltages, was carefully obtained at 0.1 K when the measured dI/dV showed significant differences from that of the previous step.

3. Results

In the early stage of the process, the device was undergoing a current annealing process [14]. Passing a large current through the suspended graphene enables its temperature to be increased by joule heating. The fabrication residues were likely removed by the high-temperature annealing, which can be indirectly monitored by the systematic change in the gate voltage dependence.

After sufficient iterations of the process, most of the suspended graphene devices showed a large $I(V)$ gap (Fig. 1d) without pronouncedly exhibiting a quantum dot state (Fig. S2c). The SEM image of these devices shows the direct connection between the $I(V)$ gap and the constriction (Fig. 1c) [8,9,12]. Repetitive applications of this process enabled us to achieve a very extensive range of the $I(V)$ gap from 10 meV to 2 eV, depending on the number of applications [cite; to be published elsewhere]. Nevertheless, we found a very interesting response to the high bias voltage exposure in a highly disordered sample which did not show sharp Dirac peak. That means the fabrication residues or other charge disorders could not be successfully removed by the current annealing. Some of highly disordered sample showed the appearance of the various stages of a quantum dot, suggesting that the formation of an isolated charge island.

We found that this subtle difference originated with the initial length of the suspended graphene device. A long (>~300 nm) graphene device exhibits electronic properties similar to those of a clean graphene device, which reveals a sharp Dirac peak near zero gate voltage. In contrast, the graphene devices with a short length (<~100 nm) show more rich transport features upon the high bias voltage exposure. We assume that the elimination of disorder can be particularly more difficult with a short initial length sample because the heat can escape relatively easily in a short channel with a wider width, as in our device; that is, the short channel prevents the graphene devices from obtaining sufficiently high temperatures for current annealing. This residual disorder might be a crucial condition to facilitate the various intriguing transport states. Most of our devices showed complex Coulomb diamond pattern in differential conductance map (Fig. S3). However, some of short channel devices showed distinct Coulomb diamond pattern (Fig. S4)

In this article, we focus on one of the particularly interesting highly disordered graphene device which showed distinct Coulomb diamond pattern. Before the process, an AFM image showed that the graphene width was 200 nm and its length between electrodes was 50 nm. A total of 137 series of controlled high bias voltage exposures were processed. The measurements show various electronic transport properties.

After the initial stage of current annealing, the Dirac peak of this device was located at a non-zero back gate voltage (Fig. S2a), indicating that a relatively large amount of charge disorder was not removed during the process. Further application of high bias voltage resulted in the gradual reduction of the minimum conductance, indicating that the conduction channel in the constricted graphene was continuously being reduced. The minimum

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