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Efficient compact model for calculating the surface potential of carbon-nanotube field-effect transistors using a curve-fitting method

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ABSTRACT

This paper presents an analytical method to compute the surface potential of ballistic metal-oxide semiconductor field-effect transistor (MOSFET)-like carbon-nanotube field-effect transistors (CNFETs). The proposed compact model considers the surface potential as functions of the carbon-nanotube diameter, gate insulator thickness, gate voltage and drain voltage. One of the advantages of this model is that there is no need to refer to the numerical model to recalculate the surface potential each time nanotube diameter or insulator thickness is changed. Instead of using a constant smoothing parameter regardless of the device size and applied bias voltages, a parameter calculated for the specific situations is employed to provide the simulation results with higher accuracy. The validity of the proposed model was verified by comparing the simulated output characteristics of three CNFETs with those of the numerical model and the previous compact model.

1. Introduction

As electronic devices become smaller, down to the nanoscale level, Si complementary metal-oxide semiconductor (CMOS) technologies are expected to approach a limit because of the short-channel effects such as drain-induced barrier lowering, reduction of the threshold voltage and increases in the subthreshold slope. Accordingly, much effort has been put into developing new materials and devices, achieving technological evolution in the sub-10-nm regime [1,2]. Among various investigations, carbon nanotubes (CNTs) are drawing attention and many research groups have fabricated carbon-nanotube field-effect transistors (CNFETs) with superior characteristics [3–5] and have modeled their device physics [6].

Models designed by considering the physical properties of CNFETs are called numerical models [7–9]. FETToy is the simulator developed based on such models [10]. Repeatedly calculating the surface potential in a self-consistent manner using numerical models is a tedious process. Thus, this method is not appropriate for software such as SPICE. For this reason, SPICE-compatible compact models considering the non-ballistic transport effects [11–13] and the ballistic transport behavior [14–20] were proposed to analytically approximate a self-consistent expression. In the compact models, the surface potential is approximated in a piecewise linear manner with the fitting parameter α. However, previously reported compact models involve a troublesome process of finding α from the numerical model to accurately calculate the surface potential every time either the value of nanotube diameter, gate insulator thickness, or drain voltage (V_{DS}) changes. To circumvent this problem, one study has reported expressions for α [16], but it only considers the dependence on the nanotube diameter and ignores the gate insulator thickness and V_{DS}. Some of the existing compact models introduce smoothing parameters to minimize the inaccuracies at the discontinuity, caused by the piecewise linear approximation of the surface potential [16–20].

In this work, a method to analytically determine the surface potential of coaxially gated single-walled semiconducting ballistic CNFETs is proposed. With this it is possible to calculate the surface potential in a simpler and easier way using the Boltzmann fitting function and the provided fitting coefficients.

2. Proposed compact model

A coaxial-gated MOSFET-like CNFET is considered in this paper due to its superior device performance over the Schottky barrier CNFET. A physical diagram of the CNTFET is shown in Fig. 1.

One of the most important steps taken when modeling the electrical characteristics of CNFETs is determining an expression for

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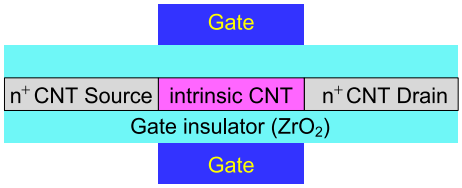

Fig. 1. Schematic cross-section of a coaxial-gated MOSFET-like CNTFET.

the surface potential as a function of the gate voltage. Neglecting the flat-band voltage, the surface potential (Ψ_s) can be expressed as:

$$\Psi_S = V_{GS} - \frac{Q_{CNT}}{C_{ins}}, \tag{1}$$

where Q_{CNT} is the total charge induced on the CNT channel surface, C_{ins} is the insulator capacitance and is given by $2\pi\epsilon_o\epsilon_{ins}/\ln(2t_{ins}/d_{CNT}+1)$ for the coaxially gated structure [19], t_{ins} is the gate insulator thickness, and d_{CNT} is the diameter of the nanotubes.

For both the numerical model and compact model, the $I-V$ characteristics of the CNFETs are determined based on the surface potential. However, the numerical models are used to calculate the surface potential in an iterative manner, while the compact models calculate it through analytic approximations as follows [14–20]:

$$\Psi_S = V_{GS} \qquad \text{for } V_{GS} < \Delta_1/q \tag{2a}$$

$$\Psi_S = V_{GS} - \alpha(V_{GS} - \Delta_1/q) \qquad \text{for } V_{GS} \geq \Delta_1/q, \tag{2b}$$

where Δ_1 is the conduction band minima of the first subband with no gate bias applied and is expressed as E_g/d_{CNT}. The parameter α in Eq. (2b) is the slope of the $V_{GS}-\Psi_S$ versus V_{GS} curve and can be expressed as a polynomial: $\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2$, where α_0, α_1 and α_2 are dependent on both the nanotube diameter and the gate insulator thickness. The piecewise linear approximation in Eq. (2) results in a discontinuity at $V_{GS} = \Delta_1/q$, where the two straight lines meet. The smoothing parameter (ϵ) was adopted in Eq. (3) to minimize the error that occurred because of the undesirable discontinuity [16–20].

$$\Psi_S = V_{GS} - \frac{\alpha\left(V_{GS} - \frac{\Delta_1}{q}\right) + \sqrt{\left\{\alpha\left(V_{GS} - \frac{\Delta_1}{q}\right)\right\}^2 + 4\epsilon^2}}{2}. \tag{3}$$

In the previously reported compact models, whenever C_{ins} or V_{DS} is changed, a new α needs to be fitted using the numerical model to obtain accurate results. Since the $V_{GS}-\Psi_S$ versus V_{GS} curve in the $V_{GS} \geq \Delta_1/q$ region is not linear, the value of α may be different depending on the chosen V_{GS}, which results in an error if the dependence of V_{GS} on α is neglected, as in the previous compact models. Hence, in this study, the surface potential was calculated without employing α and ϵ in the following way: first, the mobile charge was obtained using the FETToy simulator and substituted into Eq. (1) and the resulting surface potential was differentiated for the gate voltage. Then the $d\Psi_S/dV_{GS}$ curve was fitted with the Boltzmann function in Eq. (4a). The resultant parameters A_f, d_x and X_0 are expressed in terms of the diameter of the nanotubes and the gate insulator thickness in Eqs. (4b), (4c) and (4d), respectively.

$$\beta = A_f + \frac{A_i - A_f}{1 + e^{\frac{V_{GS}-X_0}{d_x}}}, \tag{4a}$$

$$A_f = A_0 + A_1 d_{CNT} + A_2 t_{ins} + A_3 d_{CNT}^2 + A_4 t_{ins}^2 + A_5 d_{CNT} t_{ins}, \tag{4b}$$

$$d_x = d_{x0} + d_{x1} d_{CNT} + d_{x2} t_{ins} + d_{x3} d_{CNT}^2 + d_{x4} t_{ins}^2 + d_{x5} d_{CNT} t_{ins}, \tag{4c}$$

$$X_0 = X_{00} + X_{01} d_{CNT} + X_{02} t_{ins} + X_{03} d_{CNT}^2 + X_{04} t_{ins}^2, \tag{4d}$$

where A_i and A_f are the initial and final values of $d\Psi_S/dV_{GS}$, respectively. $A_i = 1$ in this case. d_x indicates the change in V_{GS} that corresponds to the most significant change in the $d\Psi_S/dV_{GS}$ values, and X_0 is the value of V_{GS} that corresponds to the medium value between the upper and lower limits of $d\Psi_S/dV_{GS}$. The surface potential could be obtained by integrating the β value calculated from Eq. (4a), using the following expression:

$$\Psi_s = \int \beta dV_{GS}. \tag{5}$$

Since the expression for Ψ_S obtained includes the dependences on V_{DS}, V_{GS}, the nanotube diameter and the insulator thickness, it is possible that the simulation results for the proposed method will have CNFET characteristics closer to those of the numerical model than the previous compact models. In addition, the proposed method does not involve calculating the mobile charge and α from the numerical model each time either the device dimensions or V_{DS} is changed, unlike the existing compact models.

The specific voltages (ξ_S and ξ_D) for the drain current are as follows:

$$\xi_S = \frac{q\Psi_S - \Delta_1}{kT}, \tag{6a}$$

$$\xi_D = \frac{q(\Psi_S - V_{DS}) - \Delta_1}{kT}. \tag{6b}$$

The values of ξ_S and ξ_D were substituted into Eq. (7) to calculate the drain current:

$$I_{DS} = \frac{4qkT}{h}\sum[\ln\{1+\exp(-\xi_S)\} - \ln\{1+\exp(-\xi_D)\}]. \tag{7}$$

3. Results and discussion

Figs. 2 to 4 show the simulation results for a CNFET with a 2-nm-diameter carbon nanotube and a 2-nm-thick ZrO_2 gate insulator (12.1 pF/cm insulator capacitance). Fig. 2(a) shows the V_{DS} dependence of the surface potential obtained by substituting the mobile charge extracted using FETToy into Eq. (1), while Fig. 2(b) shows the derivative of the surface potential with respect to the gate voltage. For small gate voltages, the values of the surface potential were almost the same as those of the V_{GS} and thus $d\Psi_S/dV_{GS}$ was close to 1. $d\Psi_S/dV_{GS}$ decreased gradually for gate voltages near Δ_1/q and Ψ_S had a linear relationship with V_{GS} for higher gate voltages. Fig. 2(b) shows that the derivative of the surface potential with respect to the gate voltage became larger when V_{DS} increased and the gate voltage was held constant in the region where $V_{GS} > \Delta_1/q$ because of the reduced voltage drop across the gate insulator.

Fig. 3 compares the simulated $V_{GS}-\Psi_S$ curves as a function of