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Multilevel memory characteristics by light-assisted programming in floating-gate organic thin-film transistor nonvolatile memory

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ABSTRACT

In this work, we study charge trapping in floating-gate organic thin-film transistor nonvolatile memories (FG-OTFT-NVMs) fabricated by a simple method. The inner discrete distribution aluminum nanoparticles (Al-Nps) and the continuous compact thin alumina film were formed to act as the floating-gate and the tunneling dielectric layer, respectively by thermally evaporated Al at a slow rate and then heat annealed in dry air. The devices exhibited remarkable photoresponse and memory effect. Compared with the unidirectional threshold voltage (V_T) shifts of memories by programming/erasing (P/E) in dark, larger bidirectional V_T shifts were obtained by light-assisted programming, and therefore the memory performances were enhanced. A multilevel memory behavior was observed in our memories, which depended on programming conditions. The charge trapping mechanisms of memories operated in dark and under illumination are discussed, respectively. The results indicate that optimal memory performance requires charge carriers of both polarities, because it is a very efficient method to enlarge the memory window and to lower the P/E voltage by overwriting trapped charges by injected charges of opposite polarity.

1. Introduction

Flash memory devices based on the floating-gate have been widely used because massive memory capacity has been required for various applications areas. Organic memories have attracted increasing attention for their remarkable advantages such as flexibility, low-cost, large-area and easy processing. Among the many possible device configurations for organic memory, the floating-gate based on organic thin-film transistor nonvolatile memory (FG-OTFT-NVM) is considered as a promising candidate for the realization of the ultimate goal of organic flash memory because of its nonvolatile storage, nondestructive readout, complementary integrated circuit architectural compatibility, and single transistor realization [1,2]. The functionality of FG-OTFT-NVM arises from the field-effect modulation by charge carriers trapped in the floating-gate. In the FG-OTFT-NVM, both the floating-gate layer and the tunneling dielectric layer are key roles. Many kinds of nanoparticles are used to replace the conventional continuous floating-gate and to form discrete charge storage media to improve the memory performances of devices [2–8]. Thus, the formation of high-density and uniformly distributed nanoparticles is an important requirement. The high quality tunneling dielectric layer is also required. As the tunneling dielectric layer, it must be proper thin to allow controlled tunneling between the channel and the floating-gate by the proper programming/erasing (P/E) operation, and it must be compact and free-pinhole enough to inhibit the losing of the trapped charges, and it must be flat enough to facilitate the formation of good interface morphology of semiconductor/dielectric and thereby to obtain high device performances.

In this work, we demonstrated the FG-OTFT-NVM by a simple fabrication. The inner discrete distribution aluminum nanoparticles (Al-Nps) and the outer continuous compact thin alumina film were formed to act as the floating-gate and the tunneling dielectric layer, respectively. The very flat surface of the tunneling layer was obtained. The devices exhibited remarkable photoresponse and memory effect. Benefited from overwriting holes trapped in the floating-gate by injected photo-generated electrons, the clearly light-assisted programming enhanced memory characteristics were achieved in our memories. The charge trapping mechanisms of memories operated in dark and under illumination are detailed discussed, respectively.

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2. Experimental

Our FG-OTFT-NVMs were fabricated on indium tin oxide (ITO) coated glass substrates. The ITO was selectively etched to form the gate electrode. After the substrates were routinely cleaned, the gate insulator layer polymer poly-(methyl methacrylate) (PMMA) was spin-coated on the ITO gate electrode from the solution in butyl acetate, and baked at 120 °C for 3 h. The result gate insulator layer thickness was about 550 nm, measured by the Dektak 6 profiler. In the vacuum chamber at a pressure of 10^{-4} Pa, Al was thermally evaporated onto the surface of PMMA film at a slow rate of 0.1–0.3 Å/s, to form a 10 nm thick film, and patterned through a shadow mask. Next, the substrates were heat annealed at 120 °C for 3 h in a conventional oven filled with dry air. Finally, a 40 nm pentacene active layer and a 5 nm molybdenum oxidation (MoO_3)/ 60 nm Cu source-drain electrode, were thermally deposited, and patterned by the corresponding shadow masks, at the rate of about 1 Å/s, 0.3 Å/s and 2 Å/s, respectively. The result channel width (W) and length (L) was 2000 μm and 140 μm, respectively. During the deposition, the substrates were held at room temperature. A schematic diagram of the device is shown in Fig. 1(a). The electrical characteristics of the devices were measured by using two Keithley 2400 source-measure units in the dark and under illumination, respectively, at room temperature and within ambient air. For the light source, a white light-emitting diode was employed and kept at a distance of 1 cm away from the memories. The irradiation power on the memories with an intensity of 2.4 μW/cm^2 was measured by the normal silicon photodetector. The capacitance measurements were conducted with a ZL-5 model LCR analyzer.

3. Results and discussion

Fig. 1(b) shows the atomic force microscopy (AFM) image of PMMA gate insulator layer, which demonstrated that the processed PMMA film surface was very flat with a root-mean-square roughness (RMS) of 0.51 nm. The deposition rate of the active metal Al must be low for two purposes. One, Al can be partly spontaneous oxidized to form a well-proportioned mixture film of oxide and metal nanoparticles at a slow evaporation rate of 0.1–0.3 Å/s [9]. Subsequent thermal annealing made the residual metal Al on the surface of the mixture film to be completely oxidized. The compact alumina thin film can protect the inner Al-Nps from oxidation. As a result, the mixture film deposited by thermal evaporation was changed as inner discrete metal Al-Nps and outer continuous alumina film, which act as the floating-gate and the tunneling dielectric layer, respectively. Another purpose is that we hope to obtain a smooth tunneling dielectric layer surface. Basically, the charge transport in the channel takes place mainly in the first two monolayers close to the dielectric/semiconductor interface [10,11]. So, it is important to obtain a remarkable smooth tunneling dielectric layer surface, which facilitates the formation of good interface morphology of semiconductor/dielectric. Thus, it is expected to obtain high performance devices. The AFM image shown in Fig. 1(c) demonstrated that the alumina film was continuous and remarkable smooth with a RMS of 0.34 nm, which was smoother than that prepared by atomic layer deposition (ALD) [12]. Pentacene grown on this smooth alumina surface exhibited large crystallites with an average size of approximately 0.4 μm × 0.5 μm, as shown in Fig. 1(d). Benefited from this remarkable smooth tunneling dielectric layer surface, the mobility of our present

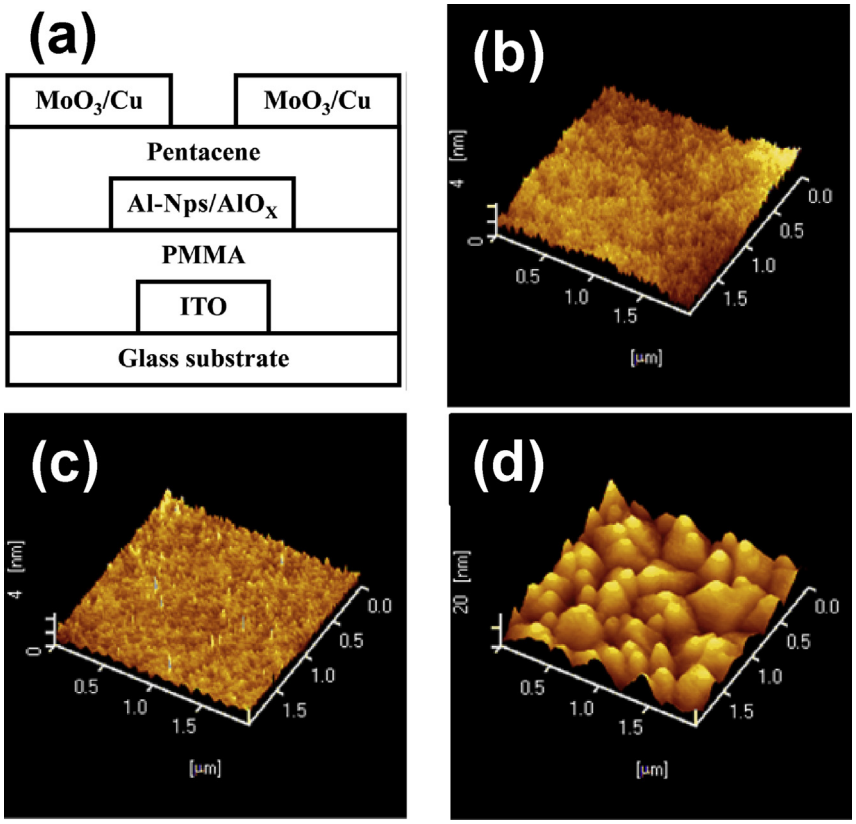

Fig. 1. (a) Schematic diagram of a floating-gate organic thin-film transistor memory. AFM images (2 μm × 2 μm) of (b) the PMMA gate insulator layer, (c) the alumina tunneling dielectric layer, and (d) the pentacene active layer deposited on the surface of alumina.