Current Applied Physics 14 (2014) 991–997

Contents lists available at ScienceDirect

Current Applied Physics

journal homepage: www.elsevier.com/locate/cap

Dielectric spectroscopy investigations of nanostructured silicon

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ARTICLE INFO

Article history:
Received 3 February 2014
Received in revised form
29 April 2014
Accepted 4 May 2014
Available online 21 May 2014

Keywords:
Broadband Dielectric Spectroscopy (BDS)
Silicon nanostructures
Relaxation processes
Metamaterial

ABSTRACT

Dielectric spectroscopy measurements were performed on planar silicon nanostructures buried within a crystalline Si that form a nanoscale Si-layered system. An insight into the specific behavior of the free-carrier population confined in the surface potential well was then made possible. It was found that the presence or the absence of the SiO_2 passivation modifies considerably relaxation responses of the studied structures. A clear differentiation of two dielectric responses: from the same sample with and without electronic passivation allowed determination of the conduction behavior in the surface c-Si delimited by the nanoscale Si-layered system. The sample with a 100 nm thick SiO_2 layer (and an excellent quality of the SiO_2/c-Si interface) exhibits a fractional power-law dielectric response, corresponding clearly to the generalized Mittag–Leffler pattern. Simultaneously, the dielectric response of a bare sample (after the total RIE of the previously deposited SiO_2 layer, about 10 nm native SiO_2 layer and poor quality of the SiO_2/c-Si interface) is dominated by the conductivity term.

1. Introduction

Semiconductor nanostructures have attracted considerable attention of the scientific community owing to their unique properties in low-dimensional physics and fabrication of nanoscale devices. Since materials science is also an important issue in solar energy conversion, an increasing number of studies particularly related to materials structured on the nanometer length scale can be found in literature [1–4]. Macroscopic characterization of semiconductor nanostructures can be used to investigate the dependence of carrier confinement and size effects on electrical, thermal and mechanical properties. On the other hand, knowledge of the influence of a given type of sample architecture would help to design and engineer more easily new materials, especially silicon-based metamaterials, with the desired properties [5–7]. Therefore, characterization techniques able to meet and control the physical properties are strongly demanded for this purpose. In particular, the electrical response to externally applied fields, which is at the basis of many properties e.g. local conductivity and dielectric behavior, is of a strong interest in micro-, nano-, opto-electronics, and solar energy conversion applications.

Dielectric relaxation spectroscopy has been widely employed to investigate the charge transport mechanism and relaxation phenomenon in semiconductors. In general, the ac electrical response of a studied material is a superposition of the dielectric response of the bound charges (dipoles) along with the hopping of the localized charge carriers and the response produced by the molecular structure deformations due to diffusion of charge carriers. The overall electric behavior can be studied by analyzing various physical quantities, i.e. complex impedance, capacitance, dielectric susceptibility and permittivity $\varepsilon^*(\omega)$ which is particularly useful to study the polarization mechanisms.

Effect of passivation on the electronic properties of silicon-based devices used for solar energy conversion is a problem discussed in many scientific publications [8]. It has been shown that a good surface passivation significantly affects the efficiency of the semiconductor wafers [9]. Using the impedance spectroscopy, it was found that the passivation process of the p–n junction does not influence the generation lifetimes but enhances the recombination lifetimes of minority carriers [10].

The objects of this research are two silicon wafers that differ with the thickness of the passivation layer SiO_2. These samples by their unique structure exhibit very interesting optical effects after a strong optical excitation [11,12]. These previously obtained dynamical results have led the authors to perform the basic electrical measurements using the dielectric spectroscopy technique.

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http://dx.doi.org/10.1016/j.cap.2014.05.004
1567-1739/

Dielectric spectroscopy measurements allow to investigate the electronic transitions between localized levels in the forbidden gap or between localized levels and the free bands. This experimental technique enables to get insight into the electronic structure of the investigated device. Moreover, it is of a great importance to analyze and understand the influence of fundamental charge relaxation processes on the electrical properties of the silicon nanostructures.

The goal of this paper is to compare electronic properties of some silicon structures containing close to the surface a nanoscale Si-layered system. Dielectric spectroscopy studies were performed on the sample covered with a good quality SiO_2 passivation layer (smooth interface) and compared with results obtained for the bare sample (poor quality interface due to the spontaneous oxidation processes leading to structural defects formation).

2. Experiment

Two samples labeled S1 and S2 originating from the same float-zone silicon wafer, that was homogeneously B-pre-doped up to 10^{15} cm^{-3}, were used in this study. Both the samples possessed the same architecture. The high quality of Si surface zone has been realized due to a homogeneous SiO_2 sacrificial oxidation of the flat (previously treated) Si surface leading to a smooth heterointerface, without inclusions or imperfections [13].

The SiO_2 sacrificial layer was etched: 80 nm layer was removed by buffer (tolerance 5%) HF solution that process 80 nm per minute; 15 nm was removed by a mixture of water and 1 mL of buffer. Then the free Si surface was covered by a 50 nm P_2O_5 layer for phosphorous (P) doping. The compensation of phosphorus doping was obtained by diffusion process performed in the so-called low temperature processing under 1000 °C (for this process at the temperature of approximately 850 °C). The inhomogeneous P doping distribution varies by two orders of magnitude along a distance of 200 nm for implanted/diffused samples.

The P^+ ion implantation was performed with 180 keV energy and the dose of about 5×10^{15} cm^{-2} through the pedestal glassy P_2O_5 nanolayer (about 5 nm remaining layer after P diffusion). The remaining P_2O_5 nanolayer protected the Si surface from the air pollution. In the S2 sample, after completing the technological processing, the P_2O_5 nanolayer was located under the SiO_2 at the SiO_2/c-Si interface. It is reasonable to assume that this pedestal layer can be at the origin of observed dipolar relaxation response in the passivated sample.

After the implantation process the samples were subjected to LPCVD (Low Pressure Chemical Vapor Deposition) oxidation, with the thickness of the SiO_2 passivation layer equal to ≈100 nm to guarantee a good quality surface with the desired electronic properties of sample S2. A surface potential well appeared in S2 sample between the SiO_2/c-Si interface and the nanoscale Si-layered system buried within the c-Si.

A schematic representation of the nanostructures used in this study is presented in Fig. 1. It should be mentioned that there is an amorphous silicon layer a-Si in the structure, embedded at a depth of about 158 nm from the c-Si/SiO_2 interface, where c-Si denotes a crystalline silicon phase and <c-Si> strained silicon layer. The two crystalline silicon (c-Si) zones next to the amorphous Si (a-Si) zone result from the solid state epitaxy during a specific thermal treatment of the buried amorphized layer resulting from the ion implantation.

In Fig. 2 results of Secondary Ion Mass Spectrometry (SIMS) measurements conducted for the S2 (passivated) sample are shown. The SIMS measurements were performed on a Cameca IMS-4f instrument. O_2^+ ions with an energy of 10 keV have been used scanning an area 1×1 mm^2. It is clear from Fig. 2 that the P_2O_5 layer is present in the sample. Moreover an extremely high density of the

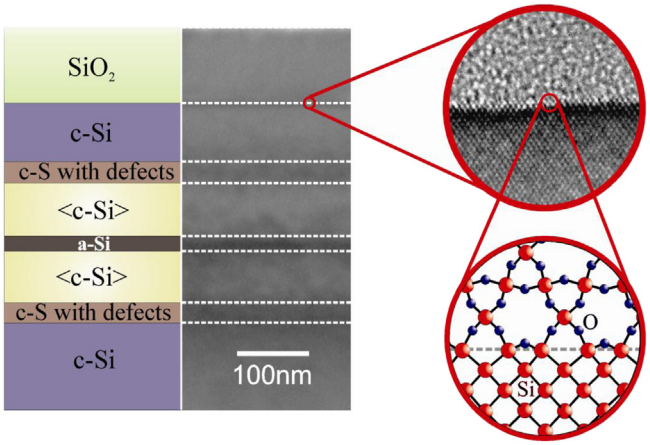

Fig. 1. Diagram of a nanoscale Si-layered system with SiO_2 cap layer. Left: identification scheme and TEM (Transmission Electron Microscope) image of the investigated silicon nanostructure. Upper right: TEM image of a SiO_2/Si interface. Lower right: drawing of the molecular structure at the interface. The inset shows a good quality SiO_2/Si interface from TEM picture and it schematic view.

confined electron gas in the superficial zone was detected. To complete the knowledge of the chemical composition in superficial strata, the SIMS profile of residual (involuntary) oxygen has been measured simultaneously.

In general, nanostructure concerns the nanoscale dimensions, 1D, 2D or 3D. In our case, the resulting multi-nanolayer flat structure is buried within the crystalline matter by a non-conventional thermodynamic treatment (implantation and annealing). This processing is at the origin of specific features (discussed in the following parts of the paper) by inducing tensile strain in 2D c-Si structures leading to new properties of previously heavily P-doped material.

Contrary to the S2 sample, in the S1 structure both cover passivation layers (remaining P_2O_5 and added SiO_2) have been etched by Reactive Ion Etching (RIE). RIE processing was performed with inductive coupled plasma etching machine AVI21 TEC OMEGA

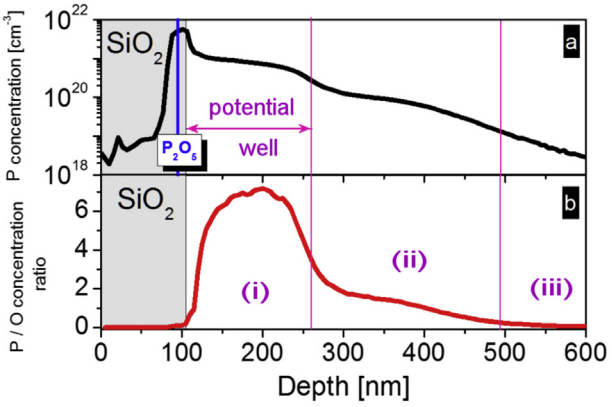

Fig. 2. Characterization of P-profile and O-profile of the S2 sample by Secondary Ion Mass Spectrometry (SIMS). (a) SIMS of the diffused/implanted wafer with its SiO_2 layer: extremely large P density in the P_2O_5 pedestal layer. (b) P/O ratio. A specific three-layer structure in the surface area of the silicon nanostructures results from the P/O ratio: i) a conducting nanolayer in the top well due to heavy P-doping only partially compensated by the involuntary O distribution; ii) an intermediate poorly conducting nanolayer due to a compensation of the heavy P-doping by the involuntary O distribution (local peak); iii) a conducting nanolayer in the bottom well due to heavy P-doping only partially compensated by the involuntary O distribution (a negligible ratio of P/O).