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The effect of annealing in forming gas on the a-IGZO thin film transistor performance and valence band cut-off of IGZO on SiNx

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ABSTRACT

In this investigation, the carrier concentration gradient between channel and contact region is achieved to improve the Thin film Transistors (TFT) performance by employing annealing at 350 °C in forming gas (N_2 + 5% H_2). The contact region is covered with Mo metal and the channel region is only exposed to forming gas to facilitate the diffusion controlled reaction. The TFT using a-IGZO active layer is fabricated in ambient of Ar:O_2 in ratio 60:40 and the conductivity of the order of 10^{-3} S/cm is measured for as-deposited sample. The electrical conductivity of an annealed sample is of the order of 10^2 S/cm. The device performance is determined by measuring merit factors of TFT. The saturation mobility of magnitude 18.5 $cm^2V^{-1}s^{-1}$ has been determined for W/L (20/10) device at 15 V drain bias. The extrapolated field effect mobility for a device with channel width (W) 10 μm is 19.3 $cm^2V^{-1}s^{-1}$. The on/off current ratio is 10^9 and threshold voltage is in the range between 2 and 3 V. The role of annealing on the electronic property of a-IGZO is carried out using X-ray photoelectron spectroscopy (XPS). The valance band cut-off has been approximately shifted to higher binding energy by 1 eV relative to as-deposited sample.

1. Introduction

Recently, Hosono et al. and H.-H. Hsu et al. have demonstrated the use of IGZO for the flexible display [1,2]. The applicability and ease of fabricating a-IGZO at room temperature has attracted attention of many researchers. Several studies have been carried out to improve the performance of TFT. The field effect mobility in various range between 10 and 68.5 $cm^2V^{-1}s^{-1}$ has been reported by several authors [2–17]. The various experimental conditions such as RF power and co-sputtering [5,10,18], oxygen partial pressure during deposition [12,19], gate oxides [1–6,9,11–14], annealing [20–23], substrate types [5,6,24] and device dimension [5–9,15,16,25–27] have been explored to improve the performance of TFT. It is to be realized that the carrier concentration has been controlled by varying oxygen's partial pressure during deposition in almost all the studies.

The device dimensions, are another important parameter that needs to be considered as it plays an important role in improving the resolution of display. In many of the reported investigations, the dimensions are too big [5–8]. To improve it, short channel devices have been demonstrated. However, the variation in the field effect mobility is marginal [9,15,16]. Kim et al. has reported a noticeable performance for small dimensional device. The high mobility of the magnitude of 35.8 $cm^2 V^{-1} s^{-1}$ has been reported for W/L (10/50) μm in [3]. However, the additional process step to form etch stopper has been employed to improve the characteristics. The highest field effect mobility of the magnitude of 68.5 $cm^2 V^{-1} s^{-1}$ has been reported for a-IGZO TFTs using the SiOx passivation and thermal-annealing treatment [10].

The performance of TFT has also been measured in term of saturation mobility as well. Moreover, the saturation mobility has been observed to be significantly smaller than the field effect mobility [28]. The saturation mobility in the range between 1 and 26.66 $cm^2 V^{-1} s^{-1}$ has been determined in various studies [28–34].

Summarizing the reported literature, reasonably good performance has been obtained for extremely higher channel length and width of TFT. Few exceptional studies have been carried out for a small dimensional device including short channel devices as well. The channel length of 6 μm, 10 μm and 50 nm devices have also

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been demonstrated in [9,15,16]. However, in those investigation, the field effect mobility exhibits in the range between 7 and 12 $cm^2 V^{-1} s^{-1}$. The high field effect mobility has been obtained for device using etch stopper of SiO_2 [3], which is due to additional process step in fabrication. Although, device dimension is relatively smaller, additional of process makes it unattractive. Thus, it is very beneficial to establish a simple process to fabricate a TFT with good performance. In this investigation, there is no addition of step, such as forming a etch stopper. It is very simple and usual process. The channel region carrier concentration is exclusively altered by annealing in forming gas and device dimension is still small. In presence of some important literature, the effect of annealing in forming gas ambient on electrical performance of a-IGZO TFT and valance band alignment on SiNx along with mechanism has yet to be studied.

In this study, the high performance transistor with very good saturation mobility, the on/off current ratio, and reasonable sub threshold swing for relatively smaller devices are proposed. The fabrication by usual process and control carrier concentration by post annealing are examined.

2. Experimental

The devices were fabricated on glass with dimensions 25×25 mm^2 using usual lithography process. The gate electrode of Mo (100 nm) was deposited using DC magnetron sputter and later was patterned out with channel width of 10, 20, 50 and 100 μm and length 10 μm followed by SiNx deposition at 300 °C using Plasma Enhanced Chemical Vapour Deposition (PECVD). The active layer of a-IGZO of 50 nm was deposited using 80 W RF power. The ambient of Ar:O_2 in the ratio of 60:40 was maintained at 5mTorr working pressure. For forming drain and source, 100 nm Mo was again deposited using DC magnetron sputtering and the electrodes were formed using wet etching process. The device was then annealed at 350 °C for an hour in forming gas ($N_2 + 5\%H_2$) ambient. The transfer characteristics were measured using main frame semiconductor analyzer E5270B. The four probe conductivity measurements at room temperature of as-deposited and annealed samples were carried out. The valance band spectra for both the sample were measured using XPS. The valance band spectra for three different a-IGZO thicknesses on SiNx 200 nm thick layer were also recorded.

The variation in the concentration of different cations between as-deposited and annealed sample suggests that the carrier concentration can be different in channel region and Source/Drain (S/D) region, as S/D is covered by 100 nm thick Mo and 20 μm in width. The ratio of concentration for various cations is provided in Table 1. On the basis of cations ratio (Ga/Zn) and In/(In + Ga + Zn), the concentration is approximately determined in the range between 7×10^{19} cm^{-3} and 1×10^{19} cm^{-3} and the Hall mobility is in the range between 9 and 20 $cm^2 V^{-1} s^{-1}$ [21].

The schematic of fabricated exposed area and covered area with 100 nm Mo metal is presented in Fig. 1 and the ideal flat band energy diagram of TFT is presented in Fig. 2.

Table 1
Ratio of concentration for various cations.

Sample SiNx(100 nm)/IGZO	Ga/Zn (1.06) [21]	Ga/(In + Ga + Zn) (0.19) [21]	In/(In+Ga+Zn) (0.62) [21]
As-dep (50 nm)	1.30	0.37	0.34
Annealed (50 nm)	0.96	0.30	0.38
As-dep (7–8 nm)	1.18	0.37	0.33
As-dep (21 nm)	1.24	0.37	0.33

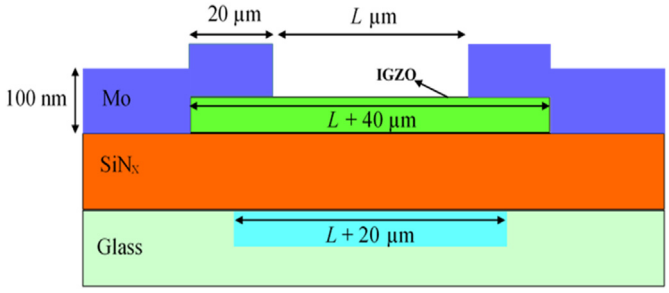

Fig. 1. Schematic with dimension of exposed area to ambient for annealing the fabricated bottom gate transistor.

3. Results and discussion

In the bottom gate TFT, the semiconducting active layer is deposited on the gate insulator. Very identical structures of films are deposited for XPS analysis. However, the IGZO thickness has been varied and valance band spectra for three different samples have been recorded. The valance spectra for the as-deposited sample (50 nm), annealed sample (50 nm), as deposited samples with thickness 7, 21 and 50 nm IGZO on SiN_x are provided in Fig. 3 (a) and (b). The variation in the valance band cut-off is clearly visible. In addition, the difference in the cut-off for the as-deposited and annealed sample is closed to 1 eV. Thus, it suggests that annealing is required to form distinct and complete valance band. The knee in valance band spectra for as-deposited sample has also been transformed to well define valance band on annealing. It has not been observed for 7 nm and 21 nm as-deposited samples. It has been suggested that O_{2p} band in UPS spectra appears in energy range 3 eV–10 eV. However due to lower cross-sectional area, these peaks may not be seen in XPS spectra. On the other hand XPS peak for vacancy appears in spectra [35–37]. Thus, the shift in valence band cut-off seems to be due to the charged oxygen and vacancy at oxygen site which results in the mid gap energy level which is visible in XPS spectra. On annealing, the unreacted oxygen or trap density decrease and the band cut-off shifted to the value of bulk IGZO. The variation in the valence band cut-off with different channel thickness is observed for as-deposited samples as shown in Fig. 3(b). The dependence of complete valence band formation on a-IGZO thickness was being investigated. However, no clear trend has been seen. The valance band of IGZO is built of oxygen and hence spectra for O (1s) peak has been analyzed for all the four samples. The reference of C (1s peak at 284.6 eV) is provided as inset in Fig. 4(a). The detail spectra for O (1s) for as-deposited 7, 21 and 50 nm a-IGZO and the sample 50 nm a-IGZO on annealing are provided in Fig. 4(a, b and c). The two distinct peaks have been observed for all the samples. Although, for the case of 50 nm samples, the ΔBE is equal to 1.6 eV, the nature of peak on annealing is distinguishable. These two peaks in case of IGZO can be attributed two kinds of oxygen surrounding. The higher binding energy peak attributed to (Ga/Zn)–O binding [38], while the lower binding energy peak is associated with In–O binding [39].

The four probe conductivity of a-IGZO on annealing in air and in reducing ambient are observed 3×10^{-3} S/cm and 5×10^{2} S/cm, respectively. The defect reaction as shown in Eq. (1) occurs in reducing ambient leading to higher carrier concentration.

$$O^x = \frac{1}{2}O_2 + V'' + 2e^- \quad (1)$$

Further, the electron mobility is also a function of carrier concentration. The fabricated devices have also been annealed in forming gas ambient. The active region of TFT is $L + 40$ μm leaving