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Extraction of density-of-states in amorphous InGaZnO thin-film transistors from temperature stress studies

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ABSTRACT

The instability of amorphous InGaZnO (a-IGZO) thin-film transistors (TFTs) with different active layer thicknesses under temperature stress has been investigated through using the density-of-states (DOS). Interestingly, the a-IGZO TFT with 22 nm active layer thickness showed a better stability than the others, which was observed from the decrease of interfacial and semiconductor bulk trap densities. The DOS was calculated based on the experimentally-obtained activation energy (E_A), which can explain the experimental observations. We developed the high-performance Al_2O_3 TFT with 22 nm IGZO channel layer (a high mobility of 7.4 cm^2/V, a small threshold voltage of 2.8 V, a high I_{on}/I_{off} 1.8×10^7, and a small *SS* of 0.16 V/dec), which can be used as driving devices in the next-generation flat panel displays.

1. Introduction

InGaZnO (IGZO) thin-film transistors (TFTs) receive considerable attention and attract increasing research interest because of their potential application in the backplane electronics of active matrix liquid crystal displays (AMLCDs) and active matrix organic light emitting diodes (AMOLEDs) [1–3]. The TFTs using IGZO fabricated at room temperature have shown higher field effect mobility than that of conventional TFTs using hydrogenated amorphous silicon active layer [4], since they have high transparency at visible light, abundance in nature, thermal and chemical stability [5–7]. Despite the impressive progress of the device performance, the device reliability still imposes limitation to the implementation of IGZO TFTs into commercial electronic products. Thus, characterization of physical mechanisms on bias/temperature/illumination induced instabilities is significant. The subgap density-of-states (DOS) over the forbidden bandgap of the IGZO film is one of the most important determining parameters for both electrical performance and reliability characteristics [8].

As an important part of TFTs, gate insulators play a crucial role in TFT performance. In the present work, Al_2O_3 gate insulators fabricated by atomic layer deposition (ALD) have been investigated for use in TFTs because of low interfacial trap density with oxide semiconductors. Among the factors affecting the performance of TFTs, such as the type of gate insulator and channel layer, the thickness of gate insulator and channel layer, the film deposition technology, the film deposition condition, etc., some groups [9–11] reported that the channel layer thickness is the vital factor. The paper focuses on the extraction method of DOS, the effect of channel layer thickness on DOS, and the relationship between instability and DOS. TFTs with IGZO thickness of 22 nm (device A), 38 nm (device B), and 50 nm (device C) were fabricated and investigated.

2. Experiments

The IGZO TFTs with Al_2O_3 gate insulators were fabricated on the highly-doped n-Si substrate. The structure of TFTs used in this study was shown in Fig. 1.

Al_2O_3 gate insulator (150 nm) were deposited using alternating exposures of $Al(CH_3)_3$ and H_2O vapor at a deposition rate of 1 Å per cycle by ALD. $Al(CH_3)_3$ and H_2O were used as the sources of Al and O, respectively. Al_2O_3 was formed after the chemical exchange between $Al(CH_3)_3$ and H_2O:

$$2Al(CH_3)_3 + 3\,H_2O \rightarrow Al_2O_3 + 6\,CH_4 \quad (1)$$

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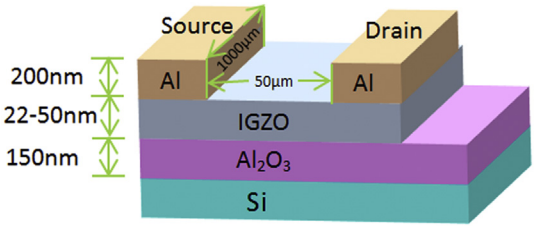

Fig. 1. Schematic structure of the IGZO-TFTs.

The temperature for ALD Al_2O_3 gate insulator deposition was fixed at 250 °C, and IGZO films were deposited by rf-magnetron sputtering at room temperature using an IGZO target (99.99%, In_2O_3, Ga_2O_3, ZnO = 1:1:1 mol%) with input power of 60 W and gas mixing ratio of Ar:O_2 (30:1). Chamber pressure before sputtering was 5×10^{-4} Pa, and total pressure was 0.5 Pa. After deposition of IGZO layer, about 200 nm Al was deposited by thermal evaporation to form the source and drain electrodes through a shadow-mask with the channel width (W) of 1000 μm and channel length (L) of 50 μm. Thermal annealing was carried out at 300 °C for 35 min in atmosphere. The thickness of the film was measured by the alpha step (Dektak 3st). The electrical characteristics of IGZO-TFTs were measured using Agilent E3647A Dual output DC power supply and Keithley 6485 Picoammeter and related software. The capacitance characteristics were measured using Agilent E4980A LRC meter. Atom force microscope (AFM, nanonaviSPA-400 SPM) was used to investigate the surface properties of films. The structural property of the films was determined using X-ray diffraction measurements with Cu-Kα radiation (D/MAX).

3. Results and discussion

Fig. 2 shows the XRD pattern of device C. The weaker peak showed in XRD result is due to the Al_2O_3/IGZO on the top of Si, which leads to a weaker X optical signal broadening received by Si. The peak appearing at 69° indicates the Si substrate. No other distinct peak is found, which means all Al_2O_3/IGZO films are amorphous in structure. Most of the advanced gate insulators studied to date are either polycrystalline or single crystal films, but it is desirable to select a material which remains in a glassy phase (amorphous) throughout the necessary processing treatments. Nearly all metal oxides of interest, with the exception of Al_2O_3, will form a polycrystalline film either during deposition or upon modest thermal treatments. Polycrystalline gate dielectrics may be problematic because grain boundaries serve as high-leakage paths, and this may lead to the need for an amorphous interfacial layer (such as Al_2O_3) to reduce leakage current [12–14]. Moreover, amorphous films have other added advantages, including low interface state density and low electronic-defect domains [15]. Therefore, using amorphous film is an effect way to suppress the leakage currents and improve the electrical properties.

Fig. 3 shows the top-view AFM image of the surface morphology of Al_2O_3 films deposited on Si. The value of root-mean-squared (RMS) roughness of Al_2O_3 films is only 0.46 nm. Thus, Al_2O_3 surface is quite smooth and uniform, which is suitable for TFT application. The smooth insulator surface could induce much less interface defects and then obtain a better channel–insulator interface [14], which combine to lead to a higher mobility and smaller sub-threshold voltage swing. Moreover, the smooth insulator surface morphology facilitates the growth of high quality IGZO film.

Fig. 4 shows corresponding transfer characteristic I_{DS} versus V_{GS} at a fixed $V_{DS} = 10$ V and the $I_{DS}^{1/2}$–V_{GS} curves of devices measured at

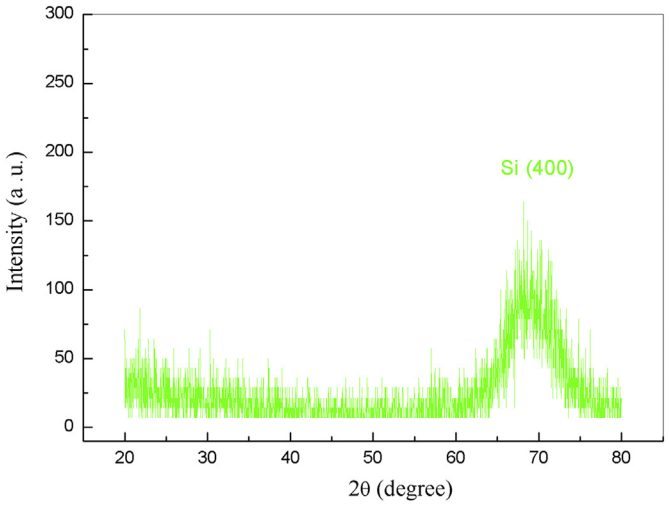

Fig. 2. XRD pattern of device C.

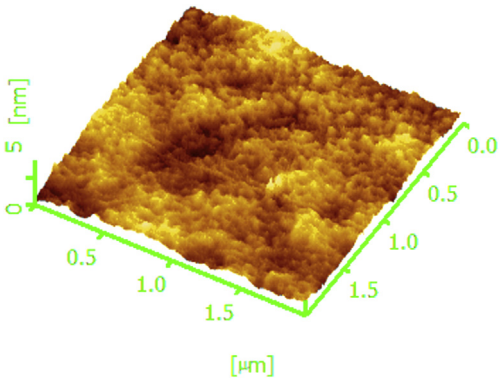

Fig. 3. The top-view AFM images of the surface morphology of Al_2O_3 films deposited on Si.

room temperature. The I_{on}/I_{off} ratios were measured at approximately 1.8×10^7, 3.5×10^7, and 3.9×10^7 for device A, B and C, respectively. This shows that these devices exhibit good characteristics as the backplane of OLEDs which require a relatively higher on-current and smaller off-current to realize rapid response and low power consumption. Based on the $I_{DS}^{1/2}$–V_{GS} curves shown in Fig. 5, field effect mobility (μ) and threshold voltage (V_{TH}) can be extracted according to the following expression:

$$I_{DS} = \frac{C_i \mu W}{2L}(V_{GS} - V_{TH})^2 \quad (\text{for } V_{DS} > V_{GS} - V_{TH}) \tag{2}$$

where C_i is the capacitance per unit area of the insulator layer (C_i is 44 nF/cm^2), W and L are the channel width and length, respectively, and V_{DS} and V_{GS} are the drain-source voltage and gate-source voltage. The field effect mobility and threshold voltage of device A, B and C were estimated at about 7.4 cm^2/V and 2.8 V, 8.6 cm^2/V and 0.7 V, and 10 cm^2/V and 0.01 V, respectively. Concerning the decrease of V_{TH} with increasing channel layer thickness (d), it was caused by the higher (absolute) number of free charges in the bulk of the thicker semiconductor, which leads to an easier accumulation of charges in the semiconductor/dielectric interface than in thinner films. This might be directly related with the existence of surface states with energies lower than the donor state energy, and as a result donor electrons become trapped at the surface (interface IGZO/Al_2O_3), leaving a region of the semiconductor next to the