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Performance improvement of amorphous indium–gallium–zinc oxide ReRAM with SiO_2 inserting layer

Yanli Pei [a, *], Biaoren Mai [a], Xiaoke Zhang [a], Ruiqin Hu [a], Ya Li [a], Zimin Chen [a], Bingfeng Fan [a], Jun Liang [b, *], Gang Wang [a]

[a] State Key Lab of Optoelectronics Materials & Technologies, School of Physics & Engineering, Sun Yat-Sen University, Guangzhou 510275, PR China
[b] Shenzhen Graduated School, Peking University, Shenzhen 518055, PR China

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ABSTRACT

In this study, the resistive switching performance of amorphous indium–gallium–zinc oxide (a-IGZO) resistive switching random-access memory (ReRAM) was improved by inserting a thin silicon oxide layer between silver (Ag) top electrode and a-IGZO resistive switching layer. Compared with the single a-IGZO layer structure, the SiO_2/a-IGZO bi-layer structure exhibits the higher On/Off resistance ratio larger than 10^3, and the lower operation power using a smaller SET compliance current. In addition, good endurance and excellent retention characteristics were achieved. Furthermore, multilevel resistance states are obtained through adjusting SET compliance current and RESET stop voltage, which shows a promise for high-performance nonvolatile multilevel memory application.

1. Introduction

Resistive random access memory (ReRAM) devices based on amorphous indium–gallium–zinc oxide (a-IGZO) are very promising for integration with a-IGZO thin film transistors (TFTs) for advanced system-on-panel (SoP) display applications with a transparent or flexible embedded system [1,2]. Therefore, it is interesting to investigate the a-IGZO ReRAM fabricated by a conventional physical deposition system at room temperature. Unfortunately, the a-IGZO-based ReRAMs present high operation current and low On/Off ratio, which limit the practical applications [3–5]. Multi-layer structures with stack engineering attract strong interests from both industry and academic to improve ReRAM performances. Wu has reported a TaO_x-based ReRAM with operational current below 10 μA by inserting a thin AlO_x barrier layer [6]. Liu has inserted Y_2O_3 layer into Pt/PrCaMnO/W ReRAM structure to obtain high On/Off ratio and low power consumption [7]. Goux has achieved sub-500 nA operation current in HfO_2-based ReRAM with Al_2O_3 barrier layer inserted between the top electrode and HfO_2 layer [8]. Lee [9] and Chen [10] have demonstrated the feasibility to increase cell endurance and to reduce power consumption by inserting a metal layer between the HfO_2 switching layer and the bottom electrode. In this work, to improve the performance of a-IGZO ReRAM, we fabricated a-IGZO ReRAM cells with a thin silicon oxide inserting layer between the top Ag electrode and a-IGZO switching layer. The characteristics of a-IGZO ReRAM devices with and without the SiO_2 insertion layer were compared and the resistive switching mechanism regarding the insertion layer was discussed.

2. Experiments

In the present work, Ti thin film of 50 nm and Pt thin film of 20 nm were successively deposited by electron beam evaporation on SiO_2/Si substrate as bottom electrode. Then, a-IGZO thin film with thickness of 40 nm was prepared on the Pt/Ti/SiO_2/Si substrate using an RF magnetron sputtering system in Ar gas ambient. The target composition is In_2O_3:Ga_2O_3:ZnO = 1:1:2. The silicon oxide insertion layer with thickness of 5 nm was deposited by RF magnetron sputtering of SiO_2 target in Ar gas ambient immediately after the a-IGZO layer deposition. All of the sputtering process steps were finished at room temperature. Finally, 160 nm-thick Ag top electrodes were deposited on the top of SiO_2 film through a shadow mask by electron beam evaporation. As reference, the ReRAMs with only a-IGZO layer were fabricated at the same condition. Fig. 1

* Corresponding authors.
E-mail addresses: peiyanli@mail.sysu.edu.cn (Y. Pei), liangjun@pkusz.edu.cn (J. Liang).

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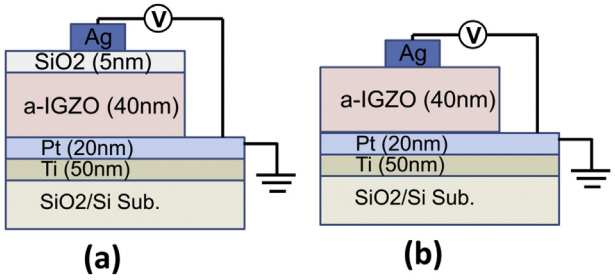

Fig. 1. Schematic structures of a-IGZO ReRAM with (a) and without (b) SiO_2 insertion layer.

shows the schematic structures of the a-IGZO ReRAMs with and without SiO_2 insertion layer. The area of top electrode was designed about 7.8×10^{-3} cm^2. The electrical performances of the ReRAM devices were measured by an Agilent B 1500A. During these measurements, bias was applied to the Ag top electrode while the bottom electrode (Pt) as ground.

3. Results and discussion

Fig. 2 shows the current–voltage (I–V) curves of forming process and typical cycles of SET/RESET for the SiO_2/a-IGZO bi-layer ReRAM device. In comparison, the SET/RESET and forming characteristics of the a-IGZO ReRAM without SiO_2 insertion layer is also shown in Fig. 2. The compliance currents (Icc) are 100 μA and 10 mA for a-IGZO ReRAM devices with and without SiO_2 insertion layer, respectively. The lowest Icc values were obtained under the stable bipolar resistive switching of these ReRAMs. The initial resistances of Ag/a-IGZO/Pt cells at 0.1 V are in the range of 10^4 ~ 10^5 Ohms. In comparison, by inserting the SiO_2 layer, the initial resistances are increased to around 10^7 ~ 10^8 Ω at 0.1 V, indicating that the SiO_2 insertion layer serves as a series resistance to reduce the off state current. Moreover, we found that for ReRAM with inserting layer, the high resistance state (HRS) after RESET operation is almost back to its original state with high resistance. Thus, the On/Off ratio was improved significantly by inserting SiO_2 layer. The On/Off ratio of SiO_2/a-IGZO bi-layer ReRAM was achieved to be 2×10^4, although the ratio was 30 for the single a-IGZO layer ReRAM device.

Operation powers during SET and RESET process were summarized in Fig. 3. The SET operation power was defined as *Pset* = *Vset* × *Icc*, and RESET operation power was defined as *Preset* = *maximum* (*I* × *V*) during RESET process. Here, 100 fresh memory cells were used to evaluate. Through inserting the SiO_2 layer, the average SET and RESET operation powers were decreased about 2 orders. The operation power is as low as 10^{-4} W.

Fig. 4 shows the retention characteristic at 85 °C for the bi-layer ReRAM device. The measurement was performed by reading back the current at −0.1 V after a set and a reset process separately. An On/Off resistance ratio larger than 10^4 was remained after 10^4 s retention at 85 °C. Fig. 5 shows the switching endurance characteristics of Ag/SiO_2/a-IGZO/Pt structure ReRAM at room temperature under the measurement of DC voltage sweep. A stable resistance switching characteristics with an On/Off resistance ratio larger than 10^3 was observed during repeated SET/RESET operations of 100 cycles.

In order to understand the resistive switching mechanisms of Ag/SiO_2/a-IGZO/Pt structure ReRAM, we plot the I–V curve using log (I) vs. log (V). As shown in Fig. 6, the I–V curve of the LRS exhibits a linearly Ohmic behavior with a slope of ~1.0. However, the conduction mechanisms of HRS are more complicated. Fitting results for the HRS suggest that the charge transport behavior is in

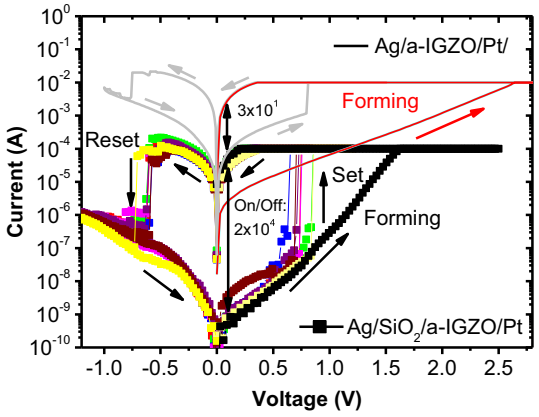

Fig. 2. Typical bipolar resistive switching I–V curves of Ag/SiO_2/a-IGZO/Pt structure with compliance current of 0.1 mA and Ag/a-IGZO/Pt structure with compliance current of 10 mA.

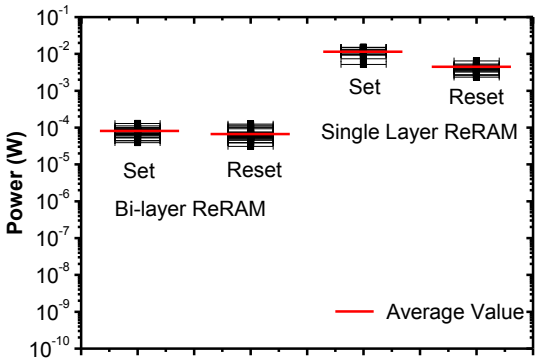

Fig. 3. SET and RESET powers of a-IGZO ReRAM devices with and without SiO_2 insertion layer.

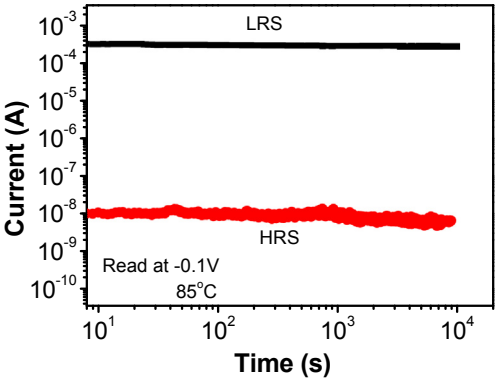

Fig. 4. Retention characteristics of LRS and HRS of Ag/SiO_2/a-IGZO/Pt structure ReRAM measured at 85 °C.

well agreement with a trap-controlled space charge limited conduction (SCLC), which mainly consists of three portions: the Ohmic region ($I \propto V$), the Child's law region ($I \propto V^2$) and the steep increase region ($I \propto V^n$, $n > 2$) [11]. The different conduction behaviors in the HRS and LRS suggest that the high conductivity in On-state cell is likely to be a confined effect rather than a homogenously distributed one. The similar I–V characteristics had been observed in the Ag/a-IGZO/Pt ReRAM structure reported in our previous work [12]. Ohmic and SCLC current are bulk dominated mechanisms. Therefore, the conductive filament resistive switching model could be