

Effect of stacked dielectric with high dielectric constant and surface modification on current enhancement in pentacene thin-film transistors

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ABSTRACT

The effect of a stacked dielectric has been studied on pentacene thin-film transistors (TFTs) with respect to the current enhancement, the crystalline polymorph, and the structural change of the film. Here we show that the performance improvement of the device is successfully achieved by the dielectric effects of the high dielectric constant and the surface modification in hybrid dielectric configuration. The systematic analysis on the device feature governed by the interfacial property was carried out for a hybrid structured insulator system using SiO₂ and cross-linked (C-L) polyvinyl alcohol (PVA), including the surface modified layer of dilute polymethyl methacrylate (PMMA). Through thickness combinations of bilayer dielectrics with low-*k* SiO₂ and high-*k* PVA, the device also exhibits noticeable enhancement of the current drivability up to the current level of 94 μ A at a practical gate bias of -30 V. Moreover, we present the effect of a surface-modified layer with dilute PMMA. After the formation of ultra-thin PMMA layer in a bilayer insulator, the organic dielectric shows an effectively changed surface property into hydrophobicity even on a strong hydroxyl-rich dielectric surface, resulting in the distinct increase of structural order in the film due to the reduction of surface free energy.

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1. Introduction

In recent years, organic thin-film transistors (OTFTs) have attracted considerable interest due to their potential applications such as drivers for flexible displays, wireless identification tags, and sensors [1–3]. Some outset products compatible with slow-speed operation of the organic transistor back-plane have already launched in the industry and its market [3]. However, in order to visualize high-speed electronics or large integrated circuits, novel techniques to improve the electrical properties are still in high demand due to their relatively low current driving level and carrier mobility compared to Si-based field effect transistors (FETs). As a matter of fact, many efforts have been put forward over the last decade to enhance OTFT properties through a variety of trials such as doping, purification, and annealing [4,5]. However, from a realistic point of view, some presented methods are still problematic for putting into practical use in actual industry applications, due to their complex and time-costly process. For this reason, gate engineering is studied intensively and has received high interest

with respect to performance enhancement [6–9], as it might promise simple and comparable steps to that of conventional device fabrication.

From the point of view of organic gate dielectric engineering, there are two primary approaches for property enhancement in transistors. One is the material design and its assignment in the gate dielectric [6,7] and the other is the modification of the interfacial property through control of the surface wettability of the dielectric [8,9]. It is widely recognized that the materials, including high-dielectric-constant (high-*k*) characteristics, are favored for serving as the gate dielectric due to their driving of high capacitance in TFT operation. Thus, various inorganic materials were introduced in the gate insulator (Ta₂O₅, TiO₂, or YO_x etc.) to achieve increased electrical performance in TFT applications [6,7]. It is also noteworthy that a properly induced terminal group on the dielectric surface might be useful for improving the device characteristics. For interfacial control between the organic active and the dielectric, the alkyl chain functional groups predominantly formed by organosilane self-assembled monolayers (SAMs) are primarily employed to obtain high mobility and high carrier density in the channel based on the inverted staggered dielectric device [8,9].

This fact underlines that using selectively combined dielectric effects can give result in further enhancement of the dielectric's electrical properties as shown in the feasibility of the mobility

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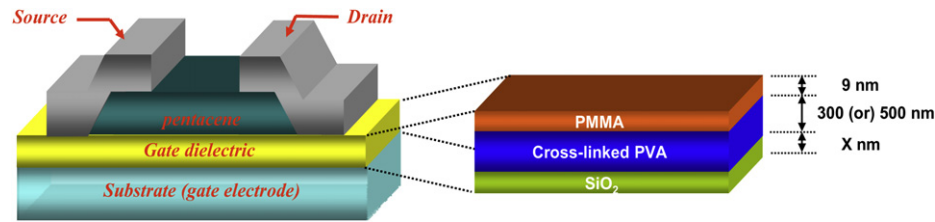


Fig. 1. Device structure of hybrid insulator OTFTs with SiO₂, cross-linked (C-L) PVA and PMMA layers. W/L = 1000/25 (μm).

improvement by employing a hybrid insulator system [10]. In this work, we provide that a systematic understanding of gate engineering on bilayer dielectrics regarding to both dielectric effects of the high dielectric constant and the surface modification from the viewpoint of the current enhancement. The surface analysis was carried out in terms of the crystalline polymorphy and the structural order of film, featured by the interface property in the stacked dielectric configuration with low-*k* inorganic SiO₂ and high-*k* organic C-L PVA polymer layer. Furthermore, we present the effect of a surface modified layer with dilute PMMA, which also identifies the successful effect of passivation and surface state alternation even on a hydroxyl-rich insulator by controlling surface free energy on the dielectric surface.

2. Experimental

Three-terminal TFTs were fabricated in top-contact geometry. The schematic of the hybrid structured device is illustrated in Fig. 1. N⁺ doped silicon wafers were used as the gate electrodes, which were thermally oxidized to various thicknesses of SiO₂ to serve as inorganic gate dielectrics. The PVA solution diluted with ammonium dichromate photosensitizer was spin-coated on the SiO₂ layers to form 500 and 300-nm thick polymer gate dielectric layers. Coated PVA layers were exposed to UV light and heated at 110 °C for about 60 min in a convection oven to make cross-linking PVA molecules and to remove water in the PVA films, respectively. For the surface modification, a PMMA layer about 9-nm thick was formed onto cross-linked PVA layers by the spin-coating process and baked at 110 °C for 60 min. Afterward, a 50-nm thick pentacene film was deposited using a thermal evaporation system, keeping the substrate temperature of 80 °C and deposition rates in the range of 0.5–1.0 Å/s. In the final step, a 50-nm thick layer of Au was thermally evaporated on top of the pentacene layer using shadow masks, producing transistors of 25 μm channel length and 1000 μm width.

The current–voltage (*I*–*V*) characteristics of the TFTs were measured with an HP 4156C semiconductor parameter analyzer in the dark. The capacitance–voltage (*C*–*V*) characteristic was also tested for capacitors by using an HP 4284A LCR meter. The dielectric constants of the cross-linked PVA and PMMA layer were estimated to be 7.8 and 3.5, respectively, from the *C*–*V* measurement at the frequency of 10 kHz, which shows similar values with previously reported ones [11–13]. The characterization of the film structure and the morphology inspection of the grown film were carried out by X-ray diffraction (XRD) using CuKα₁ radiation and atomic force microscopy (AFM), respectively.

3. Results and discussion

In contrast to many trials designed to identify high-*k* dielectric effect by employing inorganic high dielectric constant materials on an organic transistor [6,7], devices featuring a few high-*k* polymer materials as the gate insulator have been reported [14], even though they would be highly compatible with flexible application in organic electronics [1–3].

The chemical formulas of PVA and PMMA are displayed in Fig. 2(a) and (b), respectively. Among various polymer materials used in gate insulators [15], PVA is the likely candidate to serve as the gate dielectric due to its high dielectric constant characteristics with photosensitivity, flexibility, and good surface alignment effect [13,16]. The simplicity of film formation on the basis of a spin-coating process also provides comparable steps with conventional TFT processing [10]. Despite its many advantages, however, it also has a fundamental drawback in that the electrochemically rich hydroxyl (–OH) functional group, as shown in the chemical structure in Fig. 2(a), can result in a latent carrier trapping site between the pentacene/dielectric interface when it remains on the gate insulator of OTFTs [17,18], thereby making it problematic so far in putting PVA to practical use as a gate dielectric in TFT fabrication. To remove these disadvantages while preserving the advantages of PVA, a surface modification layer of PMMA containing the strong alkyl chain functional group (shown in Fig. 2(b)) was prepared as a 9-nm-thick film on a 500-nm-thick cross-linked PVA layer.

Fig. 3 shows X-ray reflectivity measurement to identify the thickness of PMMA film [9]. PMMA diluted with monochlorobenzene as the volume of 1:9 was prepared to obtain an ultra thin polymer film by the spin-coating process. The solid line indicates the best-fit curve to the experimental data as shown in violet line (in the web version) of Fig. 3. From the angular dependence of diffraction fitting curve [9,19], it clearly turns out that the ultra thin polymer layer is successfully formed as the film thickness of 9 nm. This fact reflects that an ultra thin polymer film would suppress the unfavorable low-dielectric-constant effect normally observed in the thick polymer films [15], while reserving to serve as the surface modification layer on the gate dielectric. Although the organosilane SAM formation is one of the popular manners for the surface control on the electronic device, it shows the difficulty to the practical use on the polymer surface due to its formation mechanism of hydrolysis reaction restricted on –OH tail substrate [20]. Therefore, it underlines that an ultra thin polymer layer containing the strong alkyl chain functional group can readily be available for the surface modification layer on the polymer gate insulator with providing the compatible step with the conventional TFT process.

It is worth noting that the surface property of hydrophobicity on the dielectric would be preferred to the reliable organic device operation, as it can suppress the latent trapping sites on the

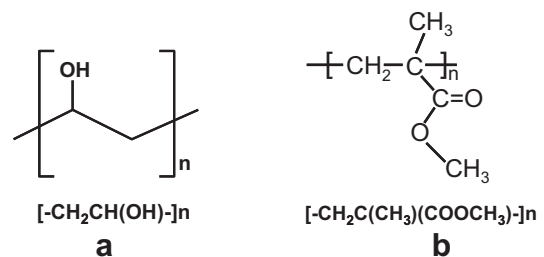


Fig. 2. Schematic diagrams of the chemical structure of (a) poly-vinyl alcohol (PVA) and (b) poly-methylmethacrylate (PMMA).

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