Storage-period dependent bias-stress instability of solution-processed amorphous indium–zinc-oxide thin-film transistors

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ABSTRACT

Storage-period dependent bias stress instability of sol–gel processed amorphous indium zinc oxide (a-InZnO) thin-film transistors (TFTs) was analyzed for more than 90 storage days. Two different solvents, 2-methoxyethnanol and acetyl acetone, were used to investigate the effect of solvent on bias-stress instability. The threshold voltage was shifted to the positive direction under positive gate-bias stress in both devices after 15 days, which is typically observed for conventional amorphous based TFTs. However, after 90 days, the TFTs became stable independent of the chemical compositions of the solvents, indicating that there is a common mechanism for solution processed a-InZnO TFTs concerning stability improvement after long storage periods. It is suggested that out-diffusion of excess oxygen in the channel region is the origin of the stable operation of a-InZnO TFTs after long storage periods.

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1. Introduction

In recent years, thin-film transistors (TFTs) based on solution-processed oxide semiconductors, because of their simple and low cost process and high throughput, have been widely studied for display and large area electronic applications [1–4]. Among the solution-based methods, the sol–gel method has attracted much attention because the composition of compound can be easily controlled, and the application of various printing methods is possible [5–7]. Up to now, several research groups have demonstrated sol–gel derived TFTs using zinc-oxide (ZnO), amorphous indium–zinc-oxide (a-InZnO), and amorphous indium–gallium–zinc-oxide (a-InGaZnO) as channel materials, showing performances comparable to that of vacuum-processed TFTs. In particular, a-InZnO semiconductor is considered a promising oxide-based channel material for high performance switching and driving device applications [8,9]. However, solution-processed a-InZnO TFTs have critical issues related to bias stress instability and reliability; these issues must be solved for the practical application of these materials in active matrix liquid crystal displays (AMLCD) or active matrix organic light-emitting diodes (AMOLED) [10,11] because charge trapping and defect creation from potential defects commonly occur during voltage and current stress measurement of amorphous based TFTs. For practical applications, long-term storage stability should be confirmed not only for simple current–voltage characteristics but also for bias-stress instability. Therefore, variations of bias stress instability for a long storage period should also be considered for the performance improvement of solution-based TFTs.

In this paper, we fabricated a-InZnO TFTs using a sol–gel process with two different solvents, 2-methoxyethnanol and acetyl acetone; we analyzed the bias stress instability as it depended on the storage period, for periods up to 90 days; samples were stored in vacuum. The long-term variations of the bias-stress instability for solution-processed a-InZnO were analyzed depending on the storage period and the solution.

2. Experimental

Two InZnO solutions were prepared by dissolving indium nitrate hydrate [$In(NO_3)\cdot xH_2O$] and zinc acetate dehydrate [$Zn(CH_3COO)_2\cdot 2H_2O$] in two different solvents, 2-methoxyethanol (device A) and acetylaceton (device B). Subsequently, mono-ethanolamine (MEA) and acetic acid (CH_3COOH) were added as sol stabilizers. The solutions were stirred for more than 48 h to improve chemical homogeneity at room temperature. We used an inverted-staggered bottom-gate structure for the solution-processed a-InZnO TFTs, as shown in Fig. 1(a). A heavily doped n-type silicon was used as the substrate and the back gate. A thermally grown silicon oxide layer (200 nm, SiO_x) was used as the

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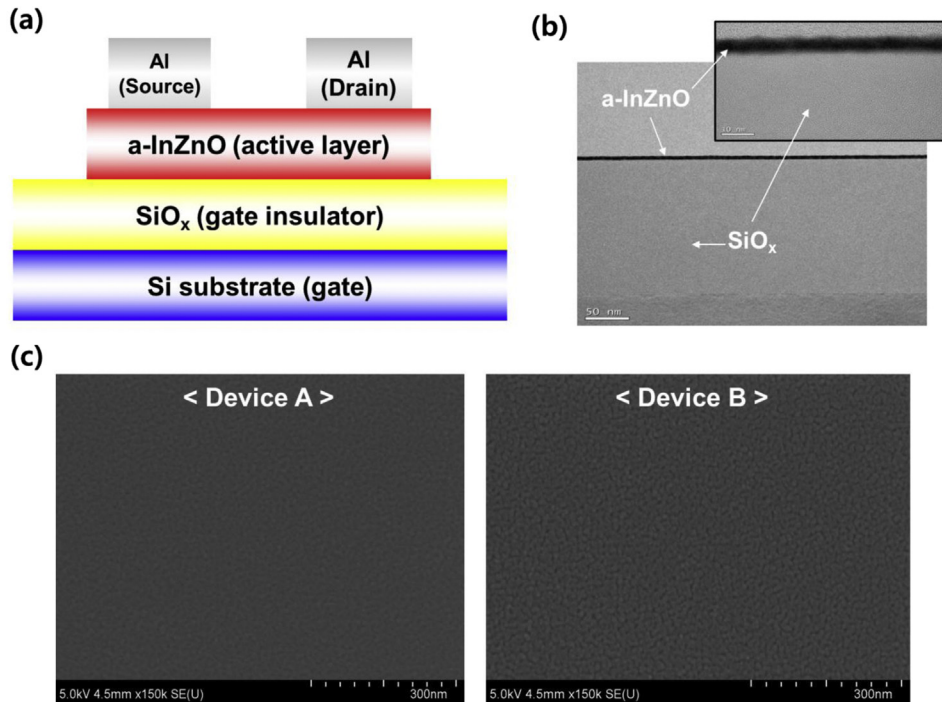*E-mail addresses:* jjeong@dgist.ac.kr, jjeong@cbnu.ac.kr (J. Jeong).

Fig. 1. (a) a-InZnO TFT structure used in this study (b) Transmission electron microscopy image of a-InZnO active layer. Scanning electron microscopy image of surface morphology for (c) device A and (d) device B.

dielectric layer. Then, the InZnO solutions were spin-coated onto the SiO$_x$/Si substrate at 5000 rpm for 30 s. After that, the films were annealed on a hot plate at 180 °C for 5 min; they were further annealed in a furnace at 500 °C for 2 h in an ambient oxygen for the thermal decomposition of the organic residues and metal salts. The thickness of the a-InZnO active layer was about 5 nm; layer had good uniformity, which can be confirmed by the high resolution transmission electron microscopy image shown in Fig. 1(b). The a-InZnO active layer forms a similar nanostructure for different solvents, as shown in the scanning electron microscopy images in Fig. 1(c) and (d). Also, these figures indicate that the fabricated a-InZnO TFTs are amorphous phase independent of the solvent. Finally, 100 nm-thick aluminum source/drain (S/D) electrodes were deposited and patterned using a shadow mask. The channel length (L) and width (W) were about 30 and 1000 μm, respectively.

The electrical characteristics of the a-InZnO TFTs were measured using a Keithley 4200-SCS semiconductor parameter analyzer at room temperature. X-ray photoelectron spectroscopy (XPS) measurements were performed to analyze the quantitative chemical properties of the a-InZnO thin films.

3. Results and discussion

Fig. 2(a) and (b) show the transfer characteristics of devices A and B for different V_{DS} values. The subthreshold slope (SS) and I_{on}/I_{off} ratio values were, respectively, about 1.3 V/dec and 10^8 A/A for device A and, 2.1 V/dec and 10^7 A/A for device B. Because SS is related with the density of states (DOS) in the sub-bandgap region, device A has a small defect density compared with that of device B in the sub-bandgap region. Also, there is a large difference in the field-effect mobility (μ) of the two devices. Device A shows a saturation field-effect mobility value of 2.67 cm^2/V, while device B shows a value of 0.86 cm^2/V. A comparison of the performance between devices A and B reveals that the initial characteristics of

the solution-processed a-InZnO TFTs depends on the type of solution; this may be due to different adhesion properties, interfacial states, or film densities of the a-InZnO thin films. Both devices exhibited good saturation behavior in the output characteristics shown in Fig. 2(c) and (d). The linear increase of the drain current in the low V_{DS} region indicates that there is no current crowding and that parasitic resistance is sufficiently low in comparison with channel resistance.

Prolonged positive gate bias stress was applied for devices A and B; variations of the threshold voltage (V_{TH}) under the gate bias stress were analyzed for 90 storage days, during which samples were stored in vacuum. Fig. 3(a) and (b) show the evolutions of the transfer characteristics for both devices under positive gate-bias stress conditions (V_{GS} = 20 V) after 15 storage days. The transfer curves of devices A and B were shifted in the positive direction with an increase in stress time, which is generally observed for various TFTs and is known to originate from charge trapping in the gate insulator [12,13]. In our case, there is a large V_{TH} shift (ΔV_{TH}) up to about 12.6 and 16.3 V for devices A and B (3600 s), respectively. However, after 90 storage days, the stabilities of devices A and B were significantly improved, as shown in Fig. 3(c) and (d). The ΔV_{TH} values of devices A and B were found to decrease to 2.0 and 5.0 V (3600 s), respectively. Though the chemical compositions of the two solvents in the a-InZnO solution were different, both devices became stable after 90 storage days. This indicates that there is a common mechanism of bias-stress instability of devices A and B concerning the improvement of stability for long storage periods. First of all, it is seen that the residual chemical components did not influence the variations of the stability of the a-InZnO TFTs for long storage periods. In addition, the charge trapping into the gate insulator is not the sole origin of the bias-stress instability of devices A and B, because the amount of defects states that can trap the electrons does not vary depending on the storage period when there is no additional treatment. Accordingly, there is another