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Nano fabricated silicon nanorod array with titanium nitride coating for on-chip supercapacitors

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ABSTRACT

We demonstrate high aspect ratio silicon nanorod arrays by cyclic deep reactive ion etching (DRIE) process as a scaffold to enhance the energy density of a Si-based supercapacitor. By unique atomic layer deposition (ALD) technology, a conformal nanolayer of TiN was deposited on the silicon nanorod arrays as the active material. The TiN coated silicon nanorods as a supercapacitor electrode lead to a 6 times improvement in capacitance compared to flat TiN film electrode.

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1. Introduction

The recent boom of Si-based micro energy harvesting systems has promoted an intense technological trend for pursuing self-powered electronic devices [1–4]. In this regard, micro energy storage systems are indispensable, as they will play a crucial role in storing and managing the harvested energy [5–8]. Electrochemical energy storage systems may be one of the best candidates due to their high energy utilization efficiency [9–11]. Currently, microbatteries are the major power source for micro electronic devices even though they suffer from poor rate performance and limited cycle life [12,13]. Supercapacitor, which represents a class of electrochemical energy storage device with high power density and excellent cycling stability, has attracted tremendous interest [14–16]. On-chip supercapacitor with in-plane thin film electrodes now is showing a pathway to replace microbattery utilized previously in microelectronic integrated circuits (IC) [17,18].

Many different materials have been considered for the tailored nanostructures for on-chip electrodes, such as polypyrrole [19,20], carbide-derived porous carbon [21], carbon nanotube forests [22], onion-like carbon [23], and graphene [24]. However, these materials are typically realized by deposition strategies that leave the underlying Si substrate unused and involve non IC compatible processes. This has stimulated development of supercapacitors based on silicon, where energy density was enhanced by nanofabricating porous silicon [25] and silicon nanowires [26,27]. However, pristine silicon nanostructures suffer from low conductivity and poor chemical stability. Different coating strategies, such as carbonization of the Si nanostructure surface [28,29] and ALD technology [30–34], have been investigated to solve these show-stopper issues, which are suitable for coating high aspect ratio structures required for supercapacitor electrodes. However, carbonization of the Si surface does not provide low resistance and this leads to limited power [28,31]. Whereas, it has been shown recently that TiN coating by ALD solves the resistance and stability issues simultaneously [30–34] resulting in performance comparable to the best graphene based devices [34]. In addition of the material studies, porous Si based supercapacitors have been combined with microelectronics [35] and solar cells [36] by joining two separate Si chips. Recently, two TiN coated porous Si electrodes and electrolyte have been also directly integrated inside a silicon chip thereby forming an in-chip supercapacitor device [34].

Grass-like silicon nanorods (Si-NR) are well-known as the unwanted nanostructured by-product generated during the DRIE of silicon [37] in IC and micro-electro-mechanical system (MEMS) technology. DRIE Si-NR has not been considered as a candidate for supercapacitor electrode because of its unpredictable structure and relatively small aspect ratio (10–50) [38]. However, the DRIE Si-NR possesses the feature of two dimensional micro/nanoarray with open channel in the vertical

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direction of the array plate. Used as the electrode scaffold, the DRIE Si-NR is favorable for fast ion diffusion in and out. In this study, taking use of the advantages of the IC compatible process and one-dimensional ion diffusion characteristic of Si-NR, we developed a high performance on-chip supercapacitor by utilizing a high aspect ratio Si-NR with well-defined array of nano structures as the electrode scaffold. The active electrodes were engineered by conformal coating nanolayer TiN on the scaffold at lower temperature instead of using carbon materials. In comparison with silicon nanowires and nanoporous Si coated with carbon material, no expensive metal catalysts, high-temperature condition in chemical vapor deposition [26,27], and electrochemical etching [25,28–34] are needed. Our proof-of-concept device demonstrates the feasibility for fabricating the on-chip supercapacitors by monolithography integration.

2. Experimental

2.1. Nanostructure fabrication

To fabricate Si-NR with well controlled nano-structure and rod density on wafer scale, we developed a cyclic DRIE route [39,40], which was performed on an inductively coupled plasma system. To obtain Si-NR with depth as high as ~20 μm, extended 75 etching cycles were performed in this study.

After machining the Si-NR on heavily boron doped Si, the pristine Si-NR went through a hydrogen smoothing step, the annealing was kept at 1100 °C for 5 min, and the flow rate of hydrogen was controlled at 40 sccm. Aluminum contact pads were fabricated at the substrate backside via thermal evaporation.

Conformal TiN films were deposited by ALD in the spirit of Refs. [30,32,34]. The ALD coating was carried out at 450 °C in a Picosun reactor Sunale R-150B using $TiCl_4$ and NH_3 as the precursors and N_2 as carrier gas. The enhanced diffusion time of the precursor gases was implemented, enabling a conformal coating of high aspect ratio Si-NR. The ALD process for 1400 cycles resulted in TiN film with sheet resistivity of approximately 47 Ω/square.

2.2. Material characterization and electrochemical measurement

A Hitachi SU-3500 scanning electron microscope (SEM) equipped with electron dispersive X-ray (EDX) analysis was used to observe the morphologies and analyze the element compositions of materials.

Three-electrode set-up was employed to study the supercapacitor behavior of fabricated working electrodes. Pt counter electrode, and Ag/AgCl (in saturated KCl) reference electrode were used for test. A Zahner IM6 electrochemical workstation was used for electrochemical measurements. Cyclic voltammogram (CV) and galvanostatic charge/discharge (GCD) measurements were conducted in 1 M Na_2SO_4 electrolyte. Electrochemical impedance spectra (EIS) were measured from 100 kHz to 100 mHz with a perturbation of 10 mV at the open circuit potential. The specific capacitance (SC) of the electrodes was calculated by integrating the reductive part of the CVs and the galvanostatic discharge curves.

3. Results and discussion

Fig. 1a reveals the uniformity of the created Si-NR by cyclic DRIE, emerging as regular nanorod arrays, vertically arranged on the Si

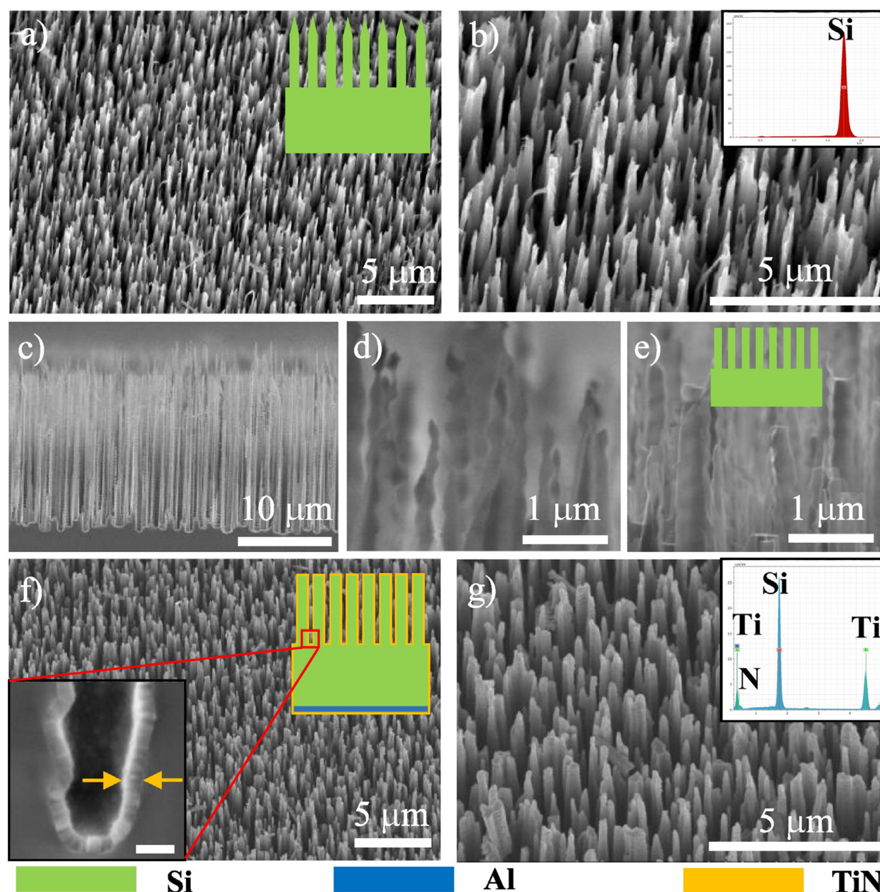

Fig. 1. SEM images: (a–b) Top view, and (c) cross-section view of pristine Si-NR. Si-NR tips before (d) and after (e) hydrogen smoothing. (f–g) Si-NR/TiN electrode. Inset sketches in (a), (e), (f) respectively illustrate the configuration of pristine Si-NR, smoothed Si-NR, Si-NR/TiN. Inset cross-section SEM image in (f) shows the TiN nano layer with ~30 nm thickness (scale bar: 50 nm). Insets in (b) and (g) display the EDX spectrums.

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