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Effects of charge storage dielectric thickness on hybrid gadolinium oxide nanocrystal and charge trapping nonvolatile memory

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ABSTRACT

The characteristics of hybrid gadolinium oxide nanocrystal (Gd_2O_3-NC) and gadolinium oxide charge trapping (Gd_2O_3-CT) memories were investigated with different Gd_2O_3 film thickness. By performing the rapid thermal annealing on Gd_2O_3 films with different thickness, the Gd_2O_3-NCs with the diameter of 6–9 nm for charge storage, surrounded by the amorphous Gd_2O_3 (α-Gd_2O_3) layer, were formed. The α-Gd_2O_3 layer was considered to be the charge trapping layer, resulting in the large memory window of Gd_2O_3-NC/CT memories with thick Gd_2O_3 film. The charge trapping energy level of the Gd_2O_3-NCs and α-Gd_2O_3 layer was extracted to be 0.16 and 0.45 eV respectively by using the temperature-dependent retention measurement. Further, after a 10^6 program/erase cycling operation, the memory with thin Gd_2O_3 film can be predicted to sustain a 94% memory window of the first cycling one while the memory with thick Gd_2O_3 film suffered from a 30% charge loss because of the traps within the α-Gd_2O_3 layer. The Gd_2O_3 film thickness of 10 nm was optimized to exhibit superior performances of the Gd_2O_3-NC/CT memory, which can be applied into the nonvolatile memory.

1. Introduction

As the charge storage capacity of the conventional floating gate (FG) nonvolatile memory increases, the feature size of the device needs to be shrunk. The scaling of the floating gate structure approaches high difficulty beyond 32 nm node technology, primarily due to the high charge leakage current resulted from the conductive poly-silicon charge storage layer and the thin tunneling oxide [1–3]. To solve this, one promising candidate is to adopt the discrete charge storage nodes like the nanocrystals (NCs) embedded in the bottom and top dielectrics for the replacement of the poly-silicon layer [4–6]. The lateral charge leakage current can be effectively suppressed by the discontinuous storage nodes, thus enhancing the immunity of the vertical leakage current through the tunneling oxide. It is reported that the NC memories can be fabricated by lots of materials and formation strategies, which have high potential to be applied in the charge storage devices by taking the advantages over the conventional FG nonvolatile memory [7,8]. Recently, the Ge and Si NCs are proposed for the nonvolatile memory use because of the simple fabrication and complementary-metal-oxide-semiconductor (CMOS) compatible process [9–11]. The metal NCs such as Au, Pt, WSi_2, and Ni embedded in the dielectric layers can exhibit long data retention owing to the high work function [12–17]. In addition, the metal-oxide NC memory fabricated by HfO_2-NCs embedded in a SiO_2 matrix have been presented to have superior memory characteristics, especially for the large memory window and good data retention and endurance properties [18,19]. It is found that the presence of charge traps within the metal-oxide NCs as well as the surrounding dielectrics can provide the high charge storage capacity, thus the high tolerance for charge loss can be achieved [20].

Previously, the gadolinium oxide nanocrystal (Gd_2O_3-NC) has been reported to be the probable candidate as nonvolatile memories [21,22]. The Gd_2O_3-NCs can be formed by rapid thermal annealing (RTA) of the Gd_2O_3 film at an optimized temperature. The crystallized Gd_2O_3 (c-Gd_2O_3) with low energy band-gap (5.44 eV) surrounded by the amorphous Gd_2O_3 (α-Gd_2O_3) layer with high energy band-gap (6.19 eV) has been found to realize the Gd_2O_3-NCs [21,23]. The band-gap offset to achieve the electrons stored in Gd_2O_3-NCs is responsible for the charge storage of Gd_2O_3-NC memories, which is different from any other NC memory proposed before [4–19]. Furthermore, the charge trapping energy level of the Gd_2O_3-NCs can be extracted from the data retention characteristics [23]. It is expected that there may be some traps within the surrounding α-Gd_2O_3 layer, and some literature pointed out that the traps within the surrounding dielectric layer will affect the reliability behaviors of the NC memories [24,25]. To solve the problem, the CF_4 plasma treatment on the Gd_2O_3-NC memory has been

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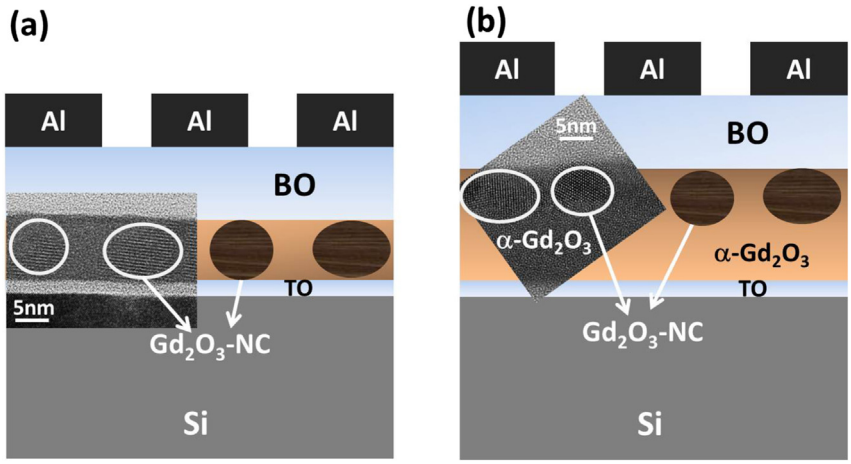

Fig. 1. Schematic structure and HRTEM image of the Gd_2O_3-NC/CT memory with the Gd_2O_3 film thickness of (a) 10 and (b) 20 nm. The tunneling oxide (TO), blocking oxide (BO), Gd_2O_3-NC, and α-Gd_2O_3 layer were indicated in the figures.

proposed to passivate the defects and modify the energy band diagram of the Gd_2O_3 film, efficiently improving the memory characteristics [25]. Nevertheless, the charge trapping characteristics of the α-Gd_2O_3 layer within the Gd_2O_3-NC memory has not yet been understood. In this paper, the thickness of the Gd_2O_3 film was varied to investigate the effect of charge storage dielectric thickness on hybrid Gd_2O_3 nanocrystal (Gd_2O_3-NC) and Gd_2O_3 charge trapping (Gd_2O_3-CT) memory. It can be found that with the increase of Gd_2O_3 film, the large memory window was obtained for the Gd_2O_3-NC/CT memory due to the thick α-Gd_2O_3 layer for charge trapping. Further, the charge trapping energy level of the α-Gd_2O_3 layer was found to be higher than that of Gd_2O_3-NCs, which will influence the memory properties such as the poor endurance characteristic of the memory with thick Gd_2O_3 layer after 10^6 program/erase (P/E) operation cycles.

2. Experimental

The Gd_2O_3-NC/CT memory devices were fabricated on 4 inch n-type (100) silicon wafers. After the standard RCA clean, a 3-nm-thick silicon dioxide film was thermally grown at 850 °C in an N_2 and O_2 mixed ambience using a horizontal furnace as the tunneling oxide. Then, the gadolinium oxide (Gd_2O_3) film was deposited on the tunneling oxide by RF sputtering with a pure gadolinium (99.9% pure) target in oxygen (O_2) and argon (Ar) mixture ambience at room temperature. The proportion of oxygen and argon ambient flow rate was 1:7, and the pressure of the chamber was 20 mtorr for amorphous Gd_2O_3 formation. The thickness of the Gd_2O_3 film was assigned to be 6, 10, 15, and 20 nm for the investigation of the charge storage dielectric thickness effect. After the charge storage dielectric films had been formed, the samples were subjected to the rapid thermal annealing (RTA) system at 900 °C for 30 s in N_2 ambient to form the Gd_2O_3-NCs surrounded by the α-Gd_2O_3 layer. Next, in order to form the blocking oxide, 8-nm-thick of SiO_2, using mixed SiH_4 and N_2O gases, was deposited using plasma enhanced chemical vapor deposition (PECVD) at 300 °C. The gas flow ratio of the SiH_4 and N_2O gases was set to be 5:200 in order to lower the deposition rate for better SiO_2 quality. After that, a 300-nm-thick aluminum (Al) film was deposited by thermal evaporator with a pure Al ingot (99.9999% pure), and a gate was defined lithographically and etched. The NC dot size of the Gd_2O_3-NC/CT memories and the film thickness of surrounding α-Gd_2O_3 layer were examined by the high resolution transmission electron microscopy (HRTEM). For the electrical analysis, the high frequency (1 MHz) capacitance–voltage (C–V) curves were measured by HP4285 precision LCR meter and the program and erase characteristics were measured by HP8110 pulse generator to supply the gate pulse.

3. Results and discussion

3.1. Material analysis and basic memory characteristics

Fig. 1(a) and (b) shows the schematic structure and the corresponding HRTEM image of the Gd_2O_3-NC/CT memories with the Gd_2O_3 film thickness of 10 and 20 nm, respectively. The crystallized Gd_2O_3-NC surrounded by the amorphous Gd_2O_3 (α-Gd_2O_3) layer can be observed in these images. The diameter of the Gd_2O_3-NCs was found to be approximately 6–9 nm regardless of the thickness of Gd_2O_3 film, which was identical to our previous study [19]. In addition, the Gd_2O_3-NCs were located at the top of the Gd_2O_3 film, which was due to the top lamp RTP system (JETFIRST 100 from AnnealSys). The heat was provided from the top of the process wafer and the Gd_2O_3-NCs were formed by the re-crystallization of the nuclei sites at the top side. Thus, large proportion of the thick Gd_2O_3 film was amorphous phase (α-Gd_2O_3) and located at the bottom of the dielectric film, as revealed in Fig. 1(b).

Fig. 2 demonstrates the capacitance–voltage (C–V) hysteresis memory window of the Gd_2O_3-NC/CT memories with different

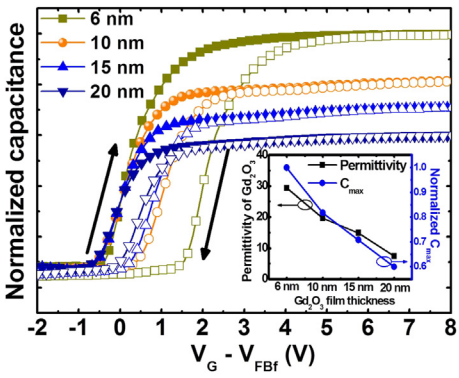

Fig. 2. High frequency C–V characteristics of the Gd_2O_3-NC/CT memories with different Gd_2O_3 film thickness. The curves were measured by sweeping the gate voltage from −13 to 13 V and then swept back. The maximum capacitance and relative permittivity of the Gd_2O_3 film were shown in the inset figure.