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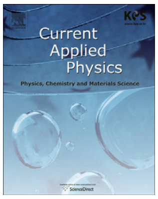

Influence of surface texturing conditions on crystalline silicon solar cell performance

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ABSTRACT

We carried out the surface texturing of crystalline silicon in alkaline solutions via anisotropic etching. We achieved random pyramids of about 10 μm in size. The size of these pyramids was then gradually reduced using a new solution. In this paper, we investigate the impact of the size of the pyramids on the emitter properties and the front electrode (Ag) contact. To make small (~3.5 μm) and large (~9.0 μm) pyramids, we controlled the texturing time and performed one-sided texturing using a silicon nitride film. We compared the formation and quality of a $POCl_3$-diffused n^+ emitter in a furnace for small and large pyramids by using SEM images and emitter saturation current density (J_{0e}) measured Quasi-Steady-State Photo-Conductance (QSSPC). For a comparison, we carried out to simulated using TCAD simulator software (SILVACO, the Athena module). After metallization, we measured the Ag contact resistance via the transfer length method (TLM). We observed the surface distributions of the Ag crystallites using SEM images. We used light *I*–*V* to measure the performance of screen-printed solar cells. The efficiency of the solar cell in the case of the small and that in the case of the large pyramids improved by about 17.4% and 17.0%, respectively. We believe that differences in the emitter uniformity and the front Ag contact resistance resulted from this difference in the cell performance. Solar cells perform better when the pyramids are small.

1. Introduction

Surface texturing is used to form highly efficient crystalline silicon solar cells. In surface texturing, anisotropic wet chemical etching is commonly used to form random pyramids by etching the rate difference in the densities of the planes in the (100) and (111) directions. It increases the short-circuit current (J_{sc}) by reducing the surface reflection loss through effective photon trapping. It is well known that textured wafers reflect 10% of the incident light while polished wafers reflect 30% [1–3]. So, surface texturing of solar cell has an impact on cell performance. These mainly study on the different kind of etchants used texturing. Recently, new surface texturing solutions have improved the surface morphology by producing small, regular pyramids [4,5].

Also, research was done on geometry of pyramids formed surface texturing. The top regions of textured pyramids form deeper junctions than do the valley regions. This is a result of the geometry of the pyramids on the textured surface, and it leads to the unevenness of the emitter region. At screen-printed Ag contact formation, causes shunt paths. These decrease the cell performance via a reduction in the open-circuit voltage (V_{oc}) and the fill factor (FF) [6,7].

In this work, we investigate the impact of the size of the pyramids on the emitter quality and the front electrode (Ag) contact. We also study the effect on cell performance.

2. Experiments

2.1. Preparation of substrates

We used p-type (100) monocrystalline silicon wafers with a diameter of 156 × 156 cm^2, a resistivity of 0.5–3.0 Ω cm, and a thickness of 200 μm. We made three different samples: S/S (front small/back small pyramids), L/S (front large/back small pyramids), and S/L (front small/back small pyramids). We formed small pyramids using a 20 wt% TMAH solution with IPA at 80 °C for 60 min. In the texturing process using the formed small pyramids, L/S and S/L samples form on the small/back as a protection mask layer using SiN_x coating. After the texturing process, the wafers are cleaned using a standard RCA cleaning procedure [8]. We used

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a hydrochloric acid and peroxide mixture (HPM, $HCl:H_2O_2:H_2O$ at 85 °C for 10 min) to remove the metal particles on the surface. We then dipped the wafers in a sulfuric acid and peroxide solution (SPM, $H_2SO_4:H_2O_2:H_2O$ at 85 °C for 10 min) to eliminate any organic material. We then eliminated the protection mask layer using a BOE solution.

We formed large pyramids using the same solution for 90 min. In addition, L/S and S/L samples evaporate on the back/small as a protection mask layer. We again performed the HPM and SPM steps, and we eliminated the protection mask layer using a BOE solution.

2.2. Emitter formation

We investigated the impact of the size of the pyramids on the emitter junction. We used wafers of small pyramids (S/S) and large pyramids (L/S) to form an n^+ emitter using $POCl_3$ diffused in a furnace. We measured the quality of the emitter via the emitter saturation current density (J_{0e}) using quasi-steady-state photo conductance (QSSPC). To see the emitter region, we deposited silicon nitride (SiN_x) onto the wafers. They were chemically etched using a mixture of $HF:HNO_3:CH_3COOH$ (1:100:25). We observed the emitter junctions using cross-sectional SEM images. For a comparison, 2-D profiles of the emitter junction were simulated using TCAD simulator software (SILVACO, the Athena module).

2.3. Metallization

The size of the pyramids has an effect on the Ag contact resistance. We measured the contact resistance via the transfer length method (TLM). After chemical etching with HNO_3, we observed the Ag crystallite distributions via SEM images. We also assessed the light I–V and pseudo I–V curves and determined that the fill factor (FF) is affected by the difference in the Ag contact resistance. We obtained the pseudo I–V using Suns-V_{oc} measurement, which is not affected by series resistance.

To analysis the Al-BSF quality under different surface conditions, we chemically etched the samples using a mixture of $HF:HNO_3:CH_3COOH$ (1:3:6). We observed the Al-BSF formation using cross-sectional SEM images. We then evaluated the quality of the BSF via the internal quantum efficiency (IQE) in the long-wavelength range (700–1000 nm). We also calculated the effective diffusion length, L_{eff}, from the IQE in the long-wavelength range (820–940 nm).

2.4. Fabrication of screen-printed solar cells

Fig. 1 shows the fabrication sequence for screen-printed solar cells (Ag/c-Si(n)/c-Si(p)/Al) for different pyramid sizes on a textured surface. A furnace used to form the emitter layer by $POCl_3$ diffusion. We then deposited silicon nitride (SiN_x), which acts as both a passivation layer and an anti-reflection coating layer, via plasma-enhanced chemical vapor deposition (PECVD). We screen-printed the front and back metal contacts using standard Ag paste and Al paste, respectively. We used the rapid thermal process (RTP) as a co-firing process. We evaluated the fabricated solar cells using light I–V measurement and IQE measurement.

3. Results and discussion

3.1. Reflectance of wafer surface

We are interested in the impact of the size of the pyramids on the performance of the solar cell. Small and large pyramids on the wafer surface are created by controlling the time of the texturing process. Fig. 2 shows SEM images of small and large pyramids on a wafer surface. Using the intercept method, we find that the size (height) of the pyramids is ∼3.5 μm (Fig. 2-(a)) and ∼9.0 μm (Fig. 2-(b)). The texturing process leads to the formation of random pyramids on the wafer surface. However, in the two samples the pyramids are clearly distinguished by size.

Pyramids on the wafer surface decrease the light reflection because the light ray traces become longer than the flat surface. As mentioned earlier, the reflectance of a textured-surface wafer is about 10%, whereas that of a flat-surface wafer is about 30%. The reflectance decreased to about 3% after the passivation deposit. The reflectance measured using a UV–visible spectrometer for wavelengths between 300 and 1100 nm. Fig. 3-(a) shows the reflectance

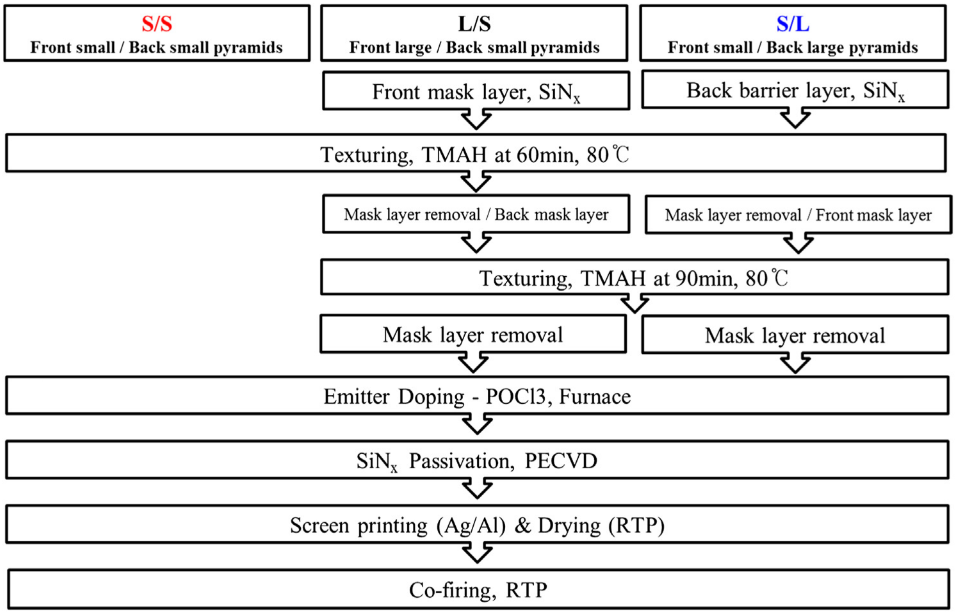

Fig. 1. Fabrication sequence of screen-printed silicon solar cells for different pyramid sizes on textured surface.