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High mechanical and electrical reliability of bottom-gate microcrystalline silicon thin film transistors on polyimide substrate

Jung-Jie Huang [a,*], Yung-Pei Chen [b], Shui-Yang Lien [a], Ko-Wei Weng [a], Ching-Hsun Chao [c]

[a] Department of Materials Science and Engineering, MingDao University, Wen-Hua Road, Peetow, Chang-Hwa 52345, Taiwan, ROC
[b] Department of Materials Science and Engineering, National Chung Hsing University, Kuo Kuang Road, Taichung, Taiwan, ROC
[c] Dow Advance Materials EM, Dow Chemical, No. 6, Kesi 2nd Rd., Chunan, Miaoli, Chunan Site, Hsinchu Science-Based Industrial Park, Taiwan, ROC

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ABSTRACT

Bottom-gate microcrystalline silicon thin film transistors (μc-Si:H TFTs) were fabricated by conventional 13.56 MHz RF plasma-enhanced chemical vapor deposition at 200 °C. In the high pressure depletion regime, the deposition rate of the μc-Si:H film is 24 nm/min and the amorphous incubation layer near the μc-Si:H/silicon nitride interface is unobvious. The crystalline fraction of μc-Si:H film with the thickness of 50 nm is 71%. From nano beam electron diffraction, the μc-Si:H film has a better crystalline order within a short-range lattice structure. The lattice parameter was measured to be 3.1 Å, which reflecting the lattice plane has a (111) direction. Finally, the μc-Si:H film was used as the active layer in TFTs structure. The field effect mobility, subthreshold swing and the threshold voltage are 0.95 cm^2/V, 0.85 V/dec. and 2.05 V, respectively. The output characteristic also shows no evidence of current crowing at low drain-source voltage (V_{ds}), implying good contact properties achieved with the n^+ a-Si:H source-drain ohmic contact layer. After 70 h 1 μA constant current stress, the threshold voltage shifts are 4.44 V and 0.42 V for the a-Si:H TFT and μc-Si:H TFT, respectively. The μc-Si:H thin film transistors show a better electrical stability than the amorphous silicon thin film transistors because of the lower defect density in the μc-Si:H film.

1. Introduction

In active matrix organic light emitting diode (AMOLED) displays, thin film transistors (TFT) are required to supply a stable drive current to each pixel. Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) can be fabricated with large areas at low cost, but they suffer from threshold voltage instability under prolonged gate voltage [1–3]. Since microcrystalline silicon (μc-Si:H) can potentially provide greater mobility and stability than the a-Si:H, it is receiving considerable attention for use in the TFT active layers of flat panel AMOLED displays [4,5].

The μc-Si:H TFT can implemented in bottom-gate and top-gate configurations. The advantage of the bottom-gate configuration is that it is an industry standard with a-Si:H TFT process. In general, bottom-gate μc-Si:H TFT has a lower mobility and poor stability, because of the presence of an amorphous incubation layer in the channel. Accordingly, ensuring that the incubation layer is very thin or absent is crucial for bottom-gate μc-Si:H TFT structures. In order to compatible with a-Si:H TFT process in industry, Direct deposition of μc-Si:H film by standard 13.56 MHz RF plasma-enhanced chemical vapor deposition (PECVD) in TFTs for AMOLED application is very attractive.

Recently, much research has been performed into a-Si:H TFTs on plastic substrates [3,6]. Curved flexible displays are produced on plastic substrates for large-area electronic applications, such as electronic paper, smart labels, sensor skin, and curved flexible displays. Plastic substrates are more flexible than glass substrates, and are lighter, thinner and more difficult to break. Therefore, studying the electrical performance of TFTs on plastic substrates is very important. However, few studies of μc-Si:H TFTs on plastic substrates have been performed. Generally, the deposition rate of a highly crystalline μc-Si:H film by PECVD is too low [7–9]. In this study, bottom-gate μc-Si:H TFTs are fabricated with a high deposition rate on a colorless 20 μm-thick polyimide substrate with a size of 37 × 47 cm^2. The transmittance of visible light ($\lambda = 550$ nm) through this substrate is 90%, as displayed in Fig. 1. Moreover, the properties of μc-Si:H TFTs on both glass and polyimide substrates are also investigated.

* Corresponding author. Tel.: +886 4 8876660x8014; fax: +886 4 8879050.
E-mail address: jjhuang@mdu.edu.tw (J.-J. Huang).

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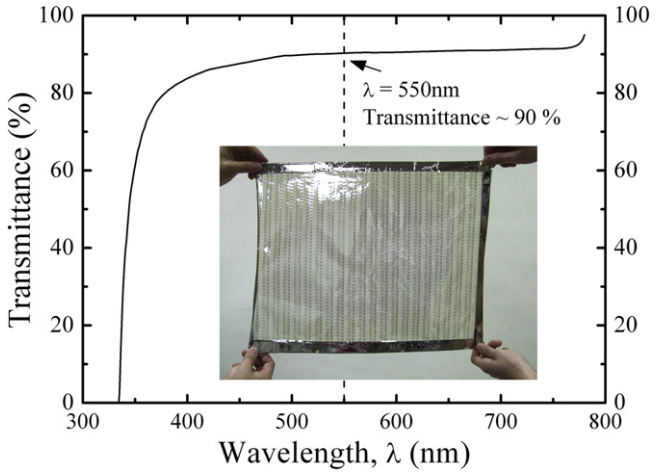

Fig. 1. Light transmittance of 20-μm-thick colorless polyimide with a size of 37 × 47 cm^2. The transmittance of visible light (λ = 550 nm) is ~90%. The inset shows a photograph of the clear polyimide substrate.

2. Device fabrication

A bottom-gate back-channel-etched (BCE) μc-Si:H TFTs structure was fabricated on both glass and polyimide substrates. Fig. 2 shows a cross-section of the μc-Si:H TFT. Its structure is the same as that of the a-Si:H TFT, but with the active layer replaced by microcrystalline silicon. The channel length and width were 3 μm and 40 μm, respectively. It was fabricated as follows. First, a Ti/Al/Ti tri-metal layer with a total thickness of 200 nm was deposited by sputtering and then patterned by dry etching to form the gate electrodes. The opposite stresses of Ti and Al compensated for their internal stresses, preventing cracking of the polyimide substrate. Then, silicon nitride, microcrystalline silicon, and n^+ a-Si:H were deposited sequentially by 13.56 MHz RF PECVD at 200 °C. The SiN_x films were deposited from a mixture of $SiH_4/NH_3/N_2/H_2$ gases (100/800/1500/1500 sccm). The working pressure and the RF power density were set at 1 torr and 0.5 W/cm^2, respectively. The μc-Si:H was deposited from a mixture of SiH_4/H_2/Ar gases (30/2700/300 sccm). The working pressure and the RF power density were set at 8 torr and 1 W/cm^2. Phosphine gas was used as a dopant source during the deposition of the n^+ a-Si:H layer. The thicknesses of the SiN_x, μc-Si:H and n^+ a-Si:H layers were 300, 200, and 50 nm, respectively. Then, an active island was formed by the island etching process. The source/drain metals were deposited and then defined by dry etching to form the source/drain electrodes. Finally, the n^+ layer between the source and drain electrodes was etched away. Following fabrication, the devices were annealed at 150 °C for 2 h to improve the source and drain contact interface.

The crystalline fraction of the microcrystalline silicon film was calculated using Raman spectroscopy, using a laser wavelength of 488 cm^{-1}. The surface morphology and roughness of the films were measured using a field emission scanning electron microscope (FE-SEM) and an atomic force microscopic (AFM), respectively. A cross-sectional high-resolution transmission electron microscopic (TEM) image was obtained. An HP-4156C semiconductor parameter analyzer was to obtain the current–voltage (*I*–*V*) characteristics at room temperature.

3. Results and discussion

Device-quality a-Si:H films have been fabricated at a deposition rate of 12 Å/s using high deposition pressure (5–10 mbar) and high RF power density (270–530 mW/cm^2) from source gas mixtures of silane and hydrogen [10]. To increase the deposition rate, the μc-Si:H films were deposited at high pressure and high power density by 13.56 MHz RF PECVD. The deposition rate of the μc-Si:H film can reach 24 nm/min, which exceeds that obtained using the same method in previous studies. Fig. 3 shows the Raman spectra of the μc-Si:H film on glass and polyimide substrates. The thickness of the μc-Si:H film was maintained at 50 nm in all samples. The Raman peak was deconvoluted using a Lorenztian multi-peak function. The crystal fraction was calculated using the formula $(I_c + I_{gb})/(I_c + I_{gb} + I_a)$ [11], where I_c, I_{gb} and I_a denote the peak areas of the crystalline, grain boundary and amorphous peaks, respectively. The crystalline fraction of the μc-Si:H film on glass and PI substrate are 71.1% and 70.6%, respectively. The Raman position of the peak from the μc-Si:H film on glass is at ~516 cm^{-1}, but that from the film on PI substrate is slightly shifted: since the latter substrate is plastic, it can release the inner stress of the film, whereas the glass substrate cannot. After the polyimide substrate had undergone 1 × 10^4 bending cycles, the crystalline fraction of the μc-Si:H film was reduced to 65.8%.

The surface morphology of the μc-Si:H films was observed by SEM and AFM as shown in Fig. 4 and Fig. 5, respectively. Fig. 4 demonstrates that the grains of the μc-Si:H films on both glass

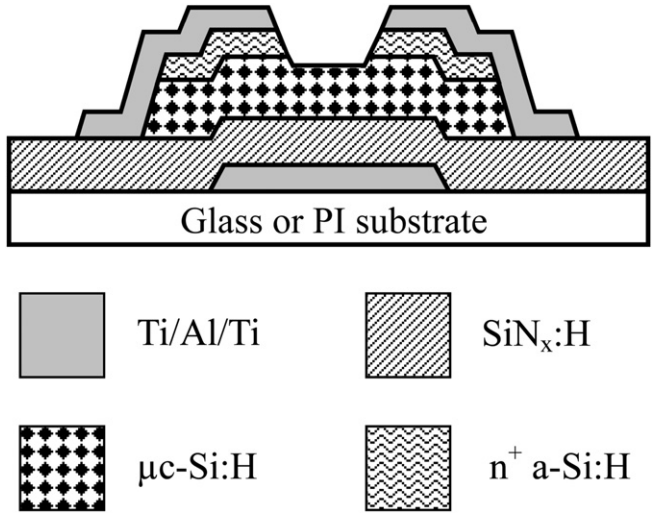

Fig. 2. Schematic cross-section view of bottom-gate μc-Si:H TFT.

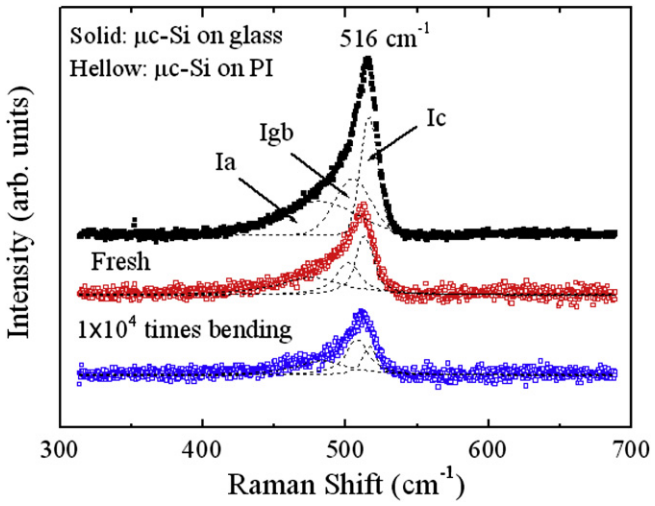

Fig. 3. Raman spectra of the μc-Si:H film on glass and polyimide substrates.