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Low power resistive random access memory using interface-engineered dielectric stack of SiO_x/a-Si/TiO_y with 1D1R-like structure

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ABSTRACT

In this study, we report a resistive random access memory (RRAM) using trilayer SiO_x/a-Si/TiO_y film structure. The low switching energy of <10 pJ, highly uniform current distribution (<13% variation), fast 50-ns speed and stable cycling endurance for 10^6 cycles are simultaneously achieved in this RRAM device. Such good performance can be ascribed to the use of interface-engineered dielectric stack with 1D1R-like structure. The SiO_x tunnel barrier in contact with top Ni electrode to form diode-like rectifying element not only lowers self-compliance switching currents, but also improves cycling endurance, which is favorable for the application of high-density 3D memory.

1. Introduction

With continued scaling down into sub-20 nm of non volatile memory (NVM), the flash NVM faces a physical limitation on charge storage in the scaled cell size [1,2]. Recently, resistive random access memories (RRAMs) [3–14] with simple metal–insulator–metal (MIM) structure and embedded function are the promising candidates for next-generation NVM. However, the large switching power and poor switching distributions are the major challenges for production. To address these issues, we have proposed low power RRAMs [11–14] based on hopping conduction mechanism [15]. Unfortunately, the current distribution related to carrier transport at the electrode/dielectric interface still cannot be well-controlled. To further improve the uniformity, 1D1R (one-diode–one-resistor) [16,17] structure is an alternative approach due to the crosstalk suppression, especially for the crossbar arrays. In this work, we adopt a novel 1D1R-like RRAM structure with good rectifying behavior to improve the switching characteristics. This RRAM device using trilayer SiO_x/a-Si/TiO_y films can achieve a low switching power of 85 μW, stable HRS/LRS ratio after repeated cycling, tight current distribution (coefficient of variation <13%) and robust pulse cycling endurance (10^6 cycles at 50 ns). The excellent switching characteristics are ascribed to the use of bilayer SiO_x/a-Si capping layer that forms a diode-like rectifying behavior (Ni/SiO_x/a-Si) to modify resistive switching characteristics of TiO_y resistor. Compared to the previous RRAM device [18] using covalent-bond oxide for uniformity improvement, the proposed low-power RRAM with 1D1R structure achieves good rectifying property to suppress the sneak current for crossbar array application. The present results show that such low-power RRAM with 1D1R-like structure design has the potential for the application of next-generation memory device.

2. Experimental procedure

First, a 200-nm-thick SiO_2 was formed on the Si substrate as a buffer layer. Then, a 100-nm-thick TaN was deposited by dc sputtering as the bottom electrodes. Next, the stacked layers of 2-nm-thick SiO_x, 6-nm-thick amorphous Si (a-Si) and 15-nm-thick TiO_y (SiO_x/a-Si/TiO_y = 2/6/15) were deposited as resistive switching layers. To investigate the switching function of each layer, we also deposit different thickness ratios of SiO_x/a-Si/TiO_y (3/6/15, 2/8/15 and 2/6/18) on bottom TaN for performance comparison. Because the thickness increase on SiO_x and a-Si layers would generate strong serial resistance effect and apparently affect the resistive switching (fast resistance window shrinking), we only select optimized thickness ratios for a fair comparison to investigate the switching mechanism and current distribution characteristics here.

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Finally, a 50-nm-thick Ni was deposited and patterned to form the top electrode by a metal mask. The schematics of fabrication process are shown in Fig. 1. All electrical characteristics of the fabricated devices were measured by an Agilent 4156 semiconductor parameter analyzer.

3. Results and discussion

For typical RRAM devices, the resistance changes from high-resistance state (HRS) to low-resistance state (LRS) during set process and returns to HRS during reset process. To study the switching characteristics of the Ni/TiO_y/TaN RRAM device, Fig. 2(a) shows the current–voltage (I–V) curve. The forming-free and self-compliance characteristics for set and reset processes are measured. The asymmetric I–V curves is originated from the different work functions of the bottom TaN (4.6 eV) and top Ni (5.1 eV) electrodes. The TiO_y RRAM device is biased at 2.5 V for set with a LRS current of 0.9 mA. For the reset process, the LRS is recovered to HRS using a bias of −2 V (36 μA). The large set current of 0.9 mA induces high power consumption and also leads to an unstable resistance switching during cycling, which is unsuitable for the requirement of low power operation. Fig. 2(b) shows the repeated cycling result after 50 cycles. During set process, the defective TiO_y with narrow bandgap generates a low barrier potential at the TiO_y/TaN interface, which induces easy formation of leakage paths and thus increases HRS current. The fast degradation of HRS current under stress leads to poor endurance. The increased HRS current with pulse cycles would result in a fast window shrinking that is not permitted for RRAM device.

To improve the performances of TiO_y RRAM, we adopted a film stack of SiO_x/a-Si on TiO_y to form a 1D1R-like memory structure. The Ni/SiO_x/a-Si acts as a doide-like rectifying element where the ultra-thin SiO_x layer is used as tunneling barrier. As shown in Fig. 3(a), the Ni/SiO_x/a-Si/TiO_y/TaN RRAM can be set and reset by different bias conditions. Although the HRS/LRS ratio read at −0.5 V becomes larger with increasing set and reset voltages from 2 V to 3 V, the tradeoff between HRS/LRS ratio and switching power needs to be considered for practical application. Moreover, the rectification behavior is clearly observed in LRS. Compared to single TiO_y RRAM, this RRAM using SiO_x/a-Si film stack with diode-like function largely lower set power from 2.3 mW to 84 μW and reset power from 72 μW to 1 μW. The improvement on switching power is due to the rectifying effect of SiO_x tunnel barrier. The rectifying 1D1R-like structure is also favorable for the fabrication of high-density crossbar array. Fig. 3(b) shows the continued cycling result after 100 cycles in Ni/SiO_x/a-Si/TiO_y/TaN RRAM. Apparently, the switching stability of HRS and LRS is much improved through the incorporation of diode-like Ni/SiO_x/a-Si structure.

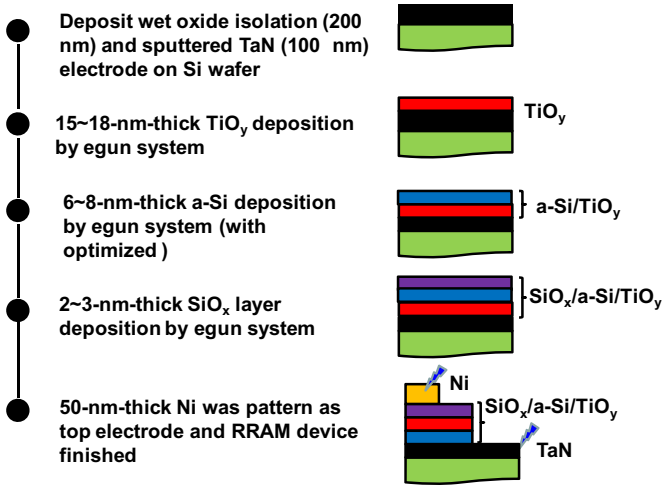

Fig. 1. Schematics of fabrication process of Ni/SiO_x/a-Si/TiO_y/TaN RRAM.

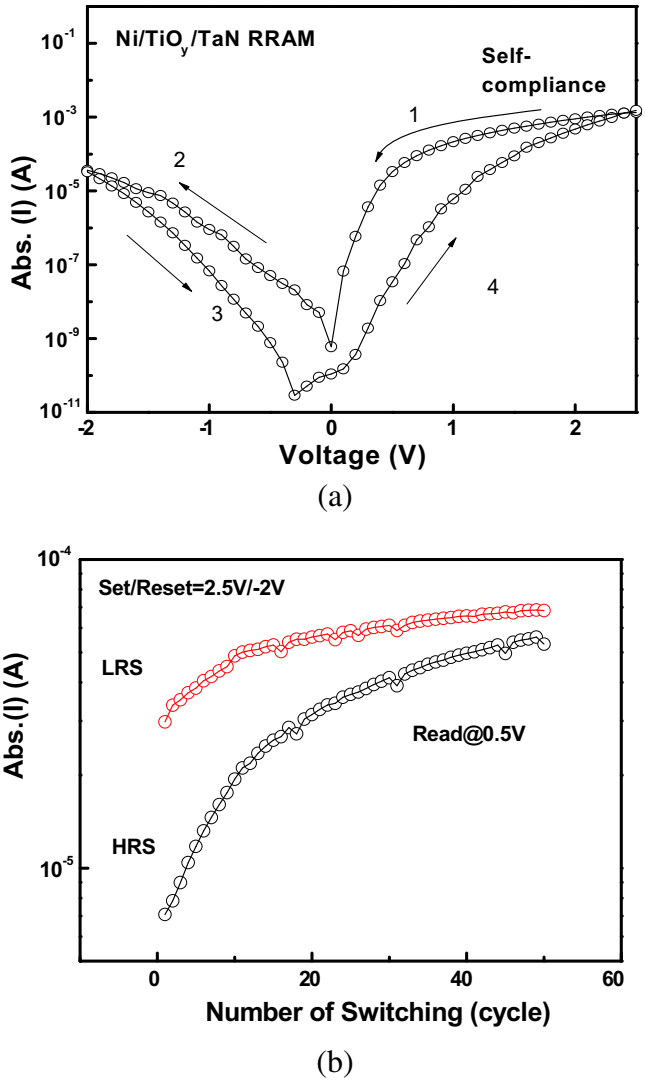

Fig. 2. (a) Swept I–V and (b) repeated cycling characteristics of Ni/TiO_y/TaN RRAM devices.

To further study the conduction mechanism, we plotted the schematic band diagrams under set and reset conditions in Fig. 4. During the set process with a positive voltage, the charged oxygen vacancies are formed via injected electrons from the bottom TaN electrode. The bottom injection of electron carriers from TaN electrode can pass through SiO_x tunnel barrier to form a LRS current. Here, the metal/tunnel barrier (Ni/SiO_x) contact plays a key role to provide the self-compliance function for set process. According to our previous research results, the low self-compliance LRS current not only lowers set power, but also improves the switching uniformity [18]. Under a negative reset bias, the SiO_x tunnel barrier with high conduction band offset forms a large potential barrier (in contact with top Ni) to break conductive paths in LRS and fast recover to HRS at a low driving power of micro-Watt. Thus, the combined effect of electrode work function tuning and interface-engineered dielectric stacks is important to reduce switching power.