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Gate stack technology for advanced high-mobility Ge-channel metal-oxide-semiconductor devices – Fundamental aspects of germanium oxides and application of plasma nitridation technique for fabrication of scalable oxynitride dielectrics

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ABSTRACT

Germanium (Ge)-based high-mobility metal-oxide-semiconductor field-effect transistors (MOSFETs) have gained considerable attention because they perform better than common Si-based devices. Although degraded electrical property of germanium oxide (GeO_2) gate insulators is considered the most serious obstacle for implementing Ge-channel for future MOSFETs, remarkable progress has been made recently. This article overviews both fundamental and technological aspects of thermally grown GeO_2, and discusses strategies for achieving ultrathin gate insulators for high-performance Ge-based MOSFETs. Our experimental and theoretical studies revealed that, despite excellent electrical property of GeO_2/Ge interface, its poor stability is a big concern, especially for ultrathin dielectrics. To overcome this problem, we investigated the impact of plasma nitridation of Ge and GeO_2 surfaces, in terms of surface cleaning, stability, and electrical properties of the nitrides. On the basis of the experimental findings, we have proposed high-quality Ge oxynitride (GeON) gate dielectrics, which consist of stable nitrogen-rich capping layers on ultrathin oxides. We implemented the GeON gate dielectrics into Ge-channel pMOSFETs and successfully demonstrated hole mobility that was 2.4 times higher than Si universal mobility.

1. Introduction

Germanium (Ge) has been used from the very beginning of semiconductor research. The world's first transistor was invented with a Ge substrate in the 1940s [1]. However, the electrical property of GeO_2/Ge system has been considered to be intrinsically poor for a number of years. In contrast, oxidation of Si surfaces produces stable SiO_2 insulators and electrical defects at SiO_2/Si interface can be effectively terminated with hydrogen atoms by a conventional forming gas annealing (FGA) treatment. These advantages of SiO_2/Si system allow us to fabricate aggressively scaled metal-oxide-semiconductor field-effect transistors (MOSFETs) [2,3]. Nowadays, hundreds of millions of Si-based MOSFETs can be integrated into a state-of-the-art microprocessor [4]. Modern integrated circuits (ICs) are manufactured at 45-nm technology node and beyond, and they use various technology boosters, such as mobility enhancement with strained Si-channel and gate leakage reduction with high-permittivity (high-k) dielectrics [5]. Although combining these technology boosters has so far enabled advanced MOSFETs to follow the technology roadmap, we now face many obstacles in Si-channel MOSFET development. There remain physical limitations of permissible channel strain and scaling of electrical thickness of gate insulator, that is, equivalent oxide thickness (EOT) scaling.

Recently, high-mobility channel materials other than strained Si-channel have been extensively investigated [6]. Compound semiconductors, such as GaAs and InGaAs, exhibit extremely high electron mobility, and thus they are possible candidate channel materials for high-performance n-channel FETs [7]. Moreover, among various semiconductors, Ge shows promise for p-channel FETs because of its highest hole mobility [8]. Considering the natures of these candidates, ultimate complementary MOS (CMOS) structure might be a combination of III–V n-channel MOSFETs and Ge p-channel MOSFETs [6]. However, such an ultimate device obviously requires both III–V/Ge hybrid structures on a Si platform and complete reassembly of the existing fabrication scheme for

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modern Si technology. In contrast, Ge is Si-compatible material that has already been implemented into mass production as a stressor for strained Si-channel [5,9]. We consider that, by taking advantage of Ge having superior hole and electron mobility to Si, Ge-CMOS is the most plausible solution for next-generation MOSFETs [10–12]. Furthermore, as theoretically suggested [13], carrier mobility of Ge-channel is expected to be further improved by introducing stress technology, just like Si technology. Therefore, it is worth re-examining fundamental aspects of Ge oxidation and electrical properties of GeO_2/Ge interface.

In this review article, we overview Ge-MOS devices and recent progress for achieving high-mobility MOS devices. This paper describes our recent theoretical and experimental studies on Ge oxidation and introduces a novel method to overcome electrical degradation of Ge-MOS devices. The second part of the article focuses on plasma nitridation of Ge and GeO_2 surfaces, in which plasma nitrogen cleaning of Ge surfaces and formation of pure Ge_3N_4 insulator are presented. On the basis of these experimental results, we developed an ultrathin Ge oxynitride (GeON) insulator with a nitride-rich capping layer and demonstrated high-mobility pMOSFETs with scaled GeON gate dielectrics.

2. Comprehensive study of GeO_2 grown on Ge

2.1. Recent progress in GeO_2/Ge system

Despite the previous belief in Ge-MOS devices, recent experimental and theoretical studies have indicated promising features of thermally grown oxides. Surprisingly, a conventional dry oxidation of Ge surfaces was found to yield an ideal GeO_2/Ge interface by choosing suitable oxidation temperatures at around 550 °C [14]. A low interface state density (D_{it}) value of less than the mid 10^{11} cm^{-2} eV^{-1} was attained without using any defect termination. According to recent theoretical predictions, this superior property of Ge-MOS devices can be attributed to the viscosity of GeO_2 to release compressive stress at the GeO_2/Ge interface [15]. Moreover, various methods other than dry oxidation, such as plasma oxidation [16], ozone oxidation [17] and high-pressure oxygen annealing [18], have been proposed. However, a drawback of GeO_2 is poor thermal stability and water solubility. According to the literature, GeO_2 decomposes at around 420 °C when it is in contact with a Ge substrate by producing volatile GeO molecules [19]. In addition, poor stability against various wet processes makes it tougher to implement Ge-channel into the conventional Si platform. Since Ge surfaces suffer from humidity in the air [20], a novel passivation technique for the Ge surface is indispensable. Furthermore, the dielectric and interface properties of Ge-MOS devices have been mainly examined for thick oxide layers (typically over 10 nm thick), and the insulating and interface qualities of GeO_2 dielectrics have not been clarified for ultrathin regions that are only a few nanometers thick required for next-generation scaled Ge-channel devices.

Nitridizing Ge surface and incorporating nitrogen into GeO_2 have received attention as a method for surface passivation and gate dielectric formation. In contrast with Si-based technology, thin oxides grown on Ge substrates by a chemical wet treatment are not applicable to a surface passivation layer [19,20]. Thus, although details of basic physical and electrical properties of Ge nitrides have not yet been fully understood, they are thought to be an alternative method to enhance compatibility of Ge-channel with the integration scheme. Moreover, pure nitride (Ge_3N_4) and oxynitride (GeON) layers are considered to be possible candidates for gate dielectrics of Ge-MOS devices [21–23]. Annealing in NH_3 ambient is a common way to incorporate nitrogen into various materials [24], but for Ge surface and GeO_2/Ge interface, the gas phase reaction usually results in unavoidable oxygen incorporation and nitrogen pile up at the interface. Previously, several groups have demonstrated that plasma nitridation is advantageous to form pure nitrides and control nitrogen profile near the surfaces [22,23], which indicate that the plasma process can develop a novel surface passivation method and stable gate dielectrics for Ge-based MOS devices.

2.2. Theoretical study on GeO_2/Ge interface

Defects at insulator/semiconductor interfaces significantly affect the performance of MOS devices. It is widely accepted that, for Si-MOS interfaces, Si dangling bonds are major electrical defects, but they are effectively terminated by hydrogen atoms with a common FGA treatment. Theoretical study on SiO_2/Si interfaces has been intensively made for decades. It is quite reasonable that, when oxygen atoms are inserted into the Si–Si network, compressive stress accumulates with the progress of oxidation. First-principles calculations of Si oxidation process have indicated that compressive stress at SiO_2/Si interface is released by emitting Si atoms from the oxidation front [25–27]. The Si-emitted structure is energetically favorable, but the resulting SiO_2/Si interface naturally involves electrical defects attributable to Si dangling bonds at the oxide interface.

As previously suggested, a low defect density at the GeO_2/Ge interface is generally explained by the smaller Young's modulus of GeO_2 than that of SiO_2 [15]. However, a detailed mechanism based on an atomistic point of view needs to be clarified. Here, we used the first-principles calculations of the GeO_2/Ge interface and compared the emission probability from the interfaces formed by oxidation of Ge and Si surfaces [28–31]. Fig. 1(a) depicts schematics of surface model for the initial oxidation. To construct GeO_2/Ge (SiO_2/Si) interface, oxygen atoms (small red circles) are inserted between a Ge–Ge network (large blue circles) whose surface is terminated with hydrogen atoms (small open circles). To examine favorable interface structure, total energy before and after atom emission was calculated on the basis of the density functional

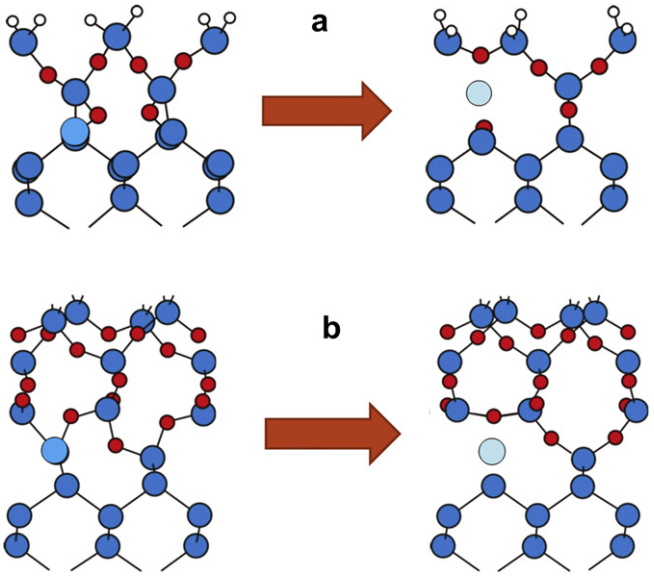

Fig. 1. Theoretical models for the first-principles calculations. (a) Initial oxidation model for Si or Ge surfaces whose uppermost dangling bonds were terminated with hydrogen atoms. (b) Interface model connected with a bulk oxide and substrate. The models on the right-hand side depict atom emission from the interface to release interface stress (see light blue circles). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)