Current Applied Physics 12 (2012) S75–S78

Contents lists available at SciVerse ScienceDirect

Current Applied Physics

journal homepage: www.elsevier.com/locate/cap

Al_2O_3/GeO_2 stacked gate dielectrics formed by post-deposition oxidation of ultrathin metal Al layer directly grown on Ge substrates

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ARTICLE INFO

Article history:
Received 30 January 2012
Received in revised form
7 March 2012
Accepted 2 April 2012
Available online 6 April 2012

Keywords:
Germanium
Alumina
High-*k* dielectric
MOS interface
High-mobility channel
Interface reaction

ABSTRACT

A simple and effective method for fabricating high-quality Al_2O_3/GeO_2 gate dielectrics is proposed. Direct deposition of ultrathin Al layers several angstroms thick on cleaned Ge surfaces followed by conventional dry oxidation was shown to form Al_2O_3/GeO_2 stacked structures. Precise control of interface GeO_2 growth was achieved due to low oxygen diffusivity in the Al_2O_3 layer. Experimental results demonstrated that, in addition to post-oxidation conditions, Al thickness is a crucial parameter for creating high-quality Ge-MOS interfaces and equivalent oxide thickness (EOT) scaling of the gate dielectrics. A correlation between electrical properties and atomic bonding features at the oxide interface was identified by multi-frequency capacitance–voltage (C–V) measurements and x-ray photoelectron spectroscopy observation. An EOT scaled down to 1.2 nm and an interface state density (D_{it}) in the lower half of the 10^{11} cm^{-2} eV^{-1} were achieved under the optimized fabrication conditions.

1. Introduction

Germanium (Ge) has recently attracted much attention and extensive study because of its higher electron and hole mobility compared to Si [1,2]. To ensure the high performance of Ge-based metal-oxide-semiconductor field-effect transistors (MOSFETs), high-quality gate insulators with scaled electrical thickness - that is, with thin equivalent oxide thickness (EOT) - are required. Germanium oxide (GeO_2) is a fundamental insulating material for Ge-MOS devices, just like SiO_2 for Si-based system. Recently, promising experimental and theoretical studies on GeO_2 insulators have been reported by several groups [3–8]. A low interface state density (D_{it}) value of less than mid 10^{11} cm^{-2} eV^{-1} is achievable with various methods, such as conventional dry oxidation [3,5], plasma oxidation [6] and high-pressure oxygen annealing [4] without using any defect termination techniques. According to theoretical predictions [7,8], this superior property of Ge-MOS interfaces can be attributed to the flexible GeO_2 network, which releases compressive stress at the interface. However, despite this superior interface quality, there are intrinsic obstacles to the implementation of high-mobility Ge channels into advanced MOSFETs: poor stability of GeO_2 and its deteriorated interface and dielectric properties, especially for the thin EOT region. It is well known that GeO_2 is water soluble and exhibits poor thermal stability [9,10], which makes it tougher to integrate Ge-MOSFETs with a Si-based platform. There have been recent demonstrations of the advantages of Ge-channels for thick oxide layers (typically over 10 nm-thick), and in fact, degraded carrier mobility has been reported for Ge-MOSFETs with ultrathin oxides [11].

Surface passivation of ultrathin GeO_2 dielectrics seems to be a plausible method for achieving scaled gate stacks while retaining the advantageous properties at the GeO_2/Ge interface. Incorporating nitrogen into GeO_2 to form GeON has been investigated as a means of improving GeO_2 stability against thermal and wet treatments [12]. We have demonstrated high-quality and stable GeON gate dielectrics with nitrogen-rich surface layers formed by plasma nitridation of ultrathin GeO_2 layers [13]. Surface-passivated GeON dielectrics provide improved stability and identical interface quality to that of thick thermal oxides, even when the EOT is scaled down to 1.7 nm. However, both the EOT and the gate leakage current need to be reduced further for next-generation Ge-based MOSFETs, meaning that high-permittivity (high-*k*) dielectrics must be combined with ultrathin GeO_2 interface layers.

Various high-*k* dielectrics have been investigated for Ge-MOS devices. In terms of typical high-*k* materials, such as Hf-based oxides and silicates, intense interface reaction and oxygen diffusion through the oxides lead to germanate formation and interface oxide growth during deposition and subsequent annealing [14]. In

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doi:10.1016/j.cap.2012.04.007

some cases, the intense reaction has a harmful impact on EOT scaling and the electrical property of the interface [14,15]. In contrast, alumina (Al_2O_3) is known to exhibit excellent stability and behave as an oxygen diffusion barrier. Previously, stacked gate dielectrics consisting of Al_2O_3 dielectrics and GeO_2 unerlayers have been examined; with these dielectrics, the atomic layer deposition (ALD) method is commonly used for Al_2O_3 growth [14,16–18]. A sufficiently low D_{it} can be achieved by carefully optimizing conditions for ALD growth and GeO_2 preparation, but further study is indispensable to ensure sufficient electrical properties, such as a low D_{it} and small hysteresis in capacitance–voltage (C–V) curves, along with an aggressively scaled EOT. As we previously reported, post-oxidation after direct high-k deposition on a cleaned Ge surface is an efficient way to form GeO_2 interface layers [19]. Recently, by taking advantage of stable Al_2O_3, successful results were obtained with ALD-Al_2O_3 growth and subsequent plasma oxidation [20,21]. However, these pioneering works require modern ALD and electron cyclotron resonance (ECR) plasma equipment and the complex two-step Al_2O_3 growth technique. In this study, we propose a very simple and effective method to fabricate high-quality Al_2O_3/GeO_2/Ge gate stacks. In the proposed method, direct deposition of an ultrathin metal Al layer on a cleaned Ge surface is performed, followed by *ex-situ* dry oxidation. Experimental results showed that the proposed method was effective in terms of ensuring a scaled EOT, small C–V hysteresis, and excellent interface properties.

2. Experimental

Fig. 1 shows a schematic illustration of the sample fabrication procedure. In our experiments, p-type Ge(100) substrates were treated with wet cleaning and then placed in an ultra-high vacuum (UHV)-based molecular beam epitaxy (MBE) system, in which thermal cleaning of Ge substrates was carried out at 500 °C for 10 min. Subsequently, ultrathin metal Al layers ranging from 0.4 to 0.8 nm were directly deposited on the cleaned Ge surface at room temperature (RT). Then, *ex-situ* dry oxidation, that is, post-deposition oxidation (PDO), was conducted at 550 °C using a conventional furnace to create Al_2O_3/GeO_2/Ge stacked structures. The ultrathin Al layer should be either partly or fully oxidized by the air exposure during transfer of the sample to the furnace. The subsequent dry oxidation enabled us to improve the insulating properties of Al_2O_3 and to precisely control the interface oxide growth owing to low oxygen diffusivity in the upper Al_2O_3 layer. Furthermore, since the GeO_2 layer is formed underneath the stable Al_2O_3 layer, we can avoid degradation of the Ge-MOS interface induced by water vapor in the air [9].

Interface oxide growth due to the dry oxidation was characterized by x-ray photoelectron spectroscopy (XPS) with a monochromated Al Kα line. We investigated the atomic bonding feature at the interfaces on the basis of a chemical shift component attributable to GeO_x interlayers by referring to our previous synchrotron photoemission experiments [22]. Au top electrodes and an Al back contact were deposited by vacuum evaporation to form Ge-MOS capacitors. The EOT versus leakage current (J_g) characteristics were derived from C–V and current–voltage (I–V) measurements. We used a low temperature conductance method to extract the D_{it} values of the Ge-MOS devices.

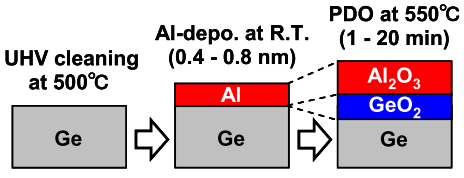

Fig. 1. Schematic illustration of fabrication procedure for Al_2O_3/GeO_2/Ge gate stacks. After Ge surface cleaning, ultrathin Al layers were directly deposited on the Ge surface at room temperature. Then, air exposure and post-deposition oxidation led to Al_2O_3 formation and interface GeO_2 growth under the optimized conditions.

3. Results and discussion

We first investigated the optimal Al thickness for fabricating Al_2O_3/GeO_2/Ge gate stacks under the given post-oxidation conditions at 550 °C for 10 min. Fig. 2(a) represents the Ge 3d core-level spectra taken after oxidation of ultrathin Al layers (0.4–0.8 nm) on Ge substrates. Binding energy position and intensity were calibrated (normalized) with the Ge bulk signal (Ge^{0+}). Intensity of the chemical shift component at a higher binding energy, corresponding to interface oxide growth, was crucially dependent on Al thickness. Thicker oxide was formed beneath the thinner Al (Al_2O_3) layer, indicating that oxygen diffusion kinetic in Al_2O_3 governs the oxide growth. Judging from the binding energy position of the chemical shift components, we can confirm the formation of stoichiometric GeO_2 interface layers for thin Al samples (0.4 and 0.6 nm). In contrast, oxidation of the Ge substrate was completely suppressed when using a 0.8 nm-thick Al layer. Note that, under the intermediate condition (Al: 0.6 nm), the chemical shift component

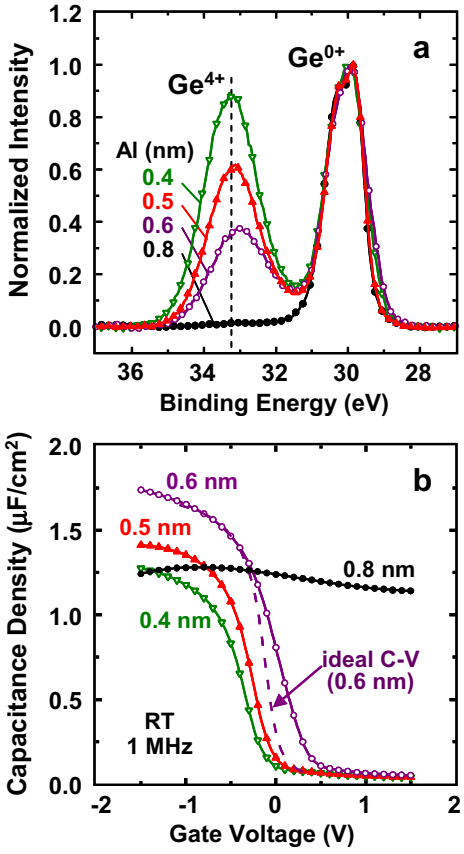

Fig. 2. Change in interface structure and electrical properties of Al_2O_3/GeO_2/p-Ge gate stacks depending on the initial metal Al thickness. Post-deposition oxidation was performed at 550 °C for 10 min for all samples. Initial Al thickness directly deposited on Ge(100) surface is indicated in the figures. (a) Ge 3d core-level spectra, in which bulk signal (Ge^{0+}) was used for both binding energy calibration and intensity normalization. (b) C–V curves taken from Ge-MOS capacitors fabricated with Au electrodes. The measurement was performed at room temperature and a frequency of 1 MHz. The ideal C–V curve for the Ge-MOS device prepared with 0.6 nm-thick Al layer is also shown.