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Relationship between interface property and energy band alignment of thermally grown SiO_2 on 4H-SiC(0001)

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ABSTRACT

Conduction band offset (ΔE_c) at SiO_2/4H-SiC(0001) interface formed by thermal oxidation in dry oxygen ambient and its modulation due to post-oxidation annealing (POA) in Ar ambient were investigated by x-ray photoelectron spectroscopy (XPS) and by electrical characterization. Valence band spectra and O 1*s* energy loss spectra taken from SiO_2/SiC structures revealed that the ΔE_c reduces with increasing POA temperature while no change in SiO_2 band gap. Capacitance–voltage (C–V) characteristics for metal-oxide-semiconductor (MOS) capacitors with as-oxidized SiO_2 gate dielectrics exhibited positive flatband voltage (V_{FB}) shift of about 2 V, hysteresis of about 1 V, and large amount of interface states (D_{it}) of the order of 10^{12} cm^{-2} eV^{-1}. High-temperature POA can improve the electrical property of SiO_2/SiC capacitors, but at the same time a reduction of ΔE_c is found in Fowler–Nordheim plots of current –voltage characteristics, which agrees with XPS analysis. V_{FB} values plotted against oxide thicknesses exhibited a linear relationship with the positive slope for both as-oxidized and 1100 °C annealed samples, indicating that negative fixed charges (Q_{it}) exist at the SiO_2/SiC interfaces. The areal densities of Q_{it} are estimated from the slopes are 1.0×10^{12} and 1.6×10^{11} cm^{-2} for as-oxidized and 1100 °C annealed samples, respectively. These results suggest that the conduction band offset at thermally grown SiO_2/SiC interface is extrinsically increased by large amount of interface charges.

1. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to replace Si-based MOSFETs to realize high-power and high-temperature applications because of its superior physical properties such as high breakdown field, high saturation drift velocity, low intrinsic carrier concentration, and high thermal conductivity. Among various wide band gap semiconductor materials, only the SiC can form chemically and thermally stable silicon dioxide (SiO_2) insulators by conventional thermal oxidation, which makes the device fabrication process easier compared with those for the other wide band gap semiconductors requiring a deposition of insulating films. Unlike the-oxidation of Si, carbon atoms in SiC must be consumed by outdiffusion of carbonate (CO) molecules from the reaction interface between SiO_2 and SiC. However, it has been reported that a small amount of carbon impurities remain at the SiO_2/SiC interface, either as isolated atoms or in the form of graphitic clusters [1,2]. Although it is still controversial whether such carbon impurities are the main cause of high-density interface defects, low current drivability due to poor channel mobility is the serious concern for SiC-MOSFETs. Therefore, several post-oxidation treatments such as high-temperature annealing in argon (Ar) [3], nitric oxide (NO_x) [4], hydrogen (H_2) [5], or phosphoryl chloride ($POCl_3$) ambient [6] have been proposed to passivate the interface defects. Furthermore, higher channel mobility was demonstrated for MOSFETs with gate oxides formed by N_2O oxidation on either 4H-SiC(000$\bar{1}$) C-face or (11$\bar{2}$ 0) a-face than that on (0001) Si-face [7].

On the other hand, conduction band offset (ΔE_c) between thermally grown SiO_2 and 4H-SiC(0001) is reported to be 2.7 eV, which is smaller than that between SiO_2 and Si (3.15 eV) [8], and apparently reduces with increasing the temperature [9]. This is a serious concern regarding gate oxide reliability because gate leakage current strongly depends on ΔE_c. Although several papers have examined ΔE_c by utilizing Fowler–Nordheim (F–N) plots of

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current–voltage (I–V) characteristics and x-ray photoelectron spectroscopy (XPS), the extracted ΔE_c values are not consistent with each other [10–15]. This may be due to the difference in an oxide formation process including post-oxidation annealing (POA) as well as to the substrate orientation. The ΔE_c at SiO_2/4H-SiC(0001) seems to be higher than that at SiO_2/4H-SiC(000$\bar{1}$) [10], and a hydrogen incorporation into SiO_2 or SiO_2/SiC interface has a tendency to decrease ΔE_c value regardless of the substrate orientation [11–14]. These results suggest that both atomic structure and fixed charge at SiO_2/SiC interface determine ΔE_c, but the relationship between interface electrical properties and ΔE_c have not been clarified yet. In this study, the energy band alignments of thermally grown SiO_2/4H-SiC(0001) structures were investigated by means of both XPS and electrical measurements of SiC-MOS capacitors. The interface property was modulated by high-temperature POA in Ar ambient (Ar-POA), and an impact of interface defect passivation on the band offset modulation at SiO_2/SiC interface was discussed.

2. Experimental

The starting substrates used in this study was 4° off-axis 4H-SiC(0001) Si-face wafers with n-type epilayer. Thin (3 nm) and thick (40 nm) SiO_2 layers were grown by thermal oxidation in dry O_2 ambient in a furnace at 1100 °C for 10 min and 12 h, respectively. Subsequently, flowing gas was changed from O_2 to Ar, and the samples were annealed at 900 or 1100 °C for 1 h. For 40-nm-thick samples, Al gate electrodes were deposited by vacuum evaporation on the oxides through a shadow mask to define MOS capacitor gates. Al was also deposited for the back contact. Capacitance–voltage (C–V) and I–V measurements were performed on the fabricated MOS capacitors. The flatband voltage (V_{FB}) and equivalent oxide thickness (EOT) were extracted from high-frequency C–V characteristics. Interface state density (D_{it}) was evaluated by high-low method and ΔE_c of SiC-MOS devices were also electrically estimated from F–N plots of the measured I–V data. The XPS measurements were performed for 3-nm-thick oxides from the oxide surfaces by using a monochromatic Al $K\alpha$ source at 1486.6 eV with a takeoff angle of 90°. To determine the energy band alignments of SiO_2/SiC structures, band gap of the SiO_2 layers and valence band offset at the interfaces were examined by XPS [16].

3. Results and discussion

Fig. 1 shows Si 2*p* core-level spectra taken from SiO_2/SiC structures with and without Ar-POA and from a reference SiC substrate. For all the oxidized samples, SiC bulk peak (Si^{0+}) and SiO_2 peak (Si^{4+}) appeared at binding energy of 101.8 eV and 104.5 eV, respectively. The difference in SiO_2 peak intensity indicates the slightly thicker oxides for Ar-POA samples. Both oxidation and Ar-POA were performed in the same furnace by changing the flowing gas from O_2 to Ar, thus oxidation could proceed to some extent during gradual replacement of O_2 by Ar in the furnace, resulting in thicker oxides for Ar-POA samples. However, the total amount of suboxide components (Si^{1+}, Si^{2+} and Si^{3+}), which appear between Si^{0+} and Si^{4+} peaks, seems to be comparable to each other. Since most of the suboxide components are considered to originate from SiO_2/SiC interface [17], structural modification of SiO_2/SiC interface by Ar-POA could not be determined from these XPS spectra. Fig. 2 shows O 1*s* energy loss spectra taken from the same samples. Since some of the photoelectrons from the sample were subjected to energy loss due to band to band excitation, energy loss spectra were observed at the higher binding energy (lower kinetic energy) from O 1*s* core-level. Energy band gap of these oxides deduced from O 1*s* energy loss spectra were identical (8.7 eV), indicating the negligible impact of Ar-POA on bulk properties of the SiO_2 layer. Fig. 3 shows valence band spectra taken from SiO_2/SiC structures with and without Ar-POA and from a reference SiC surface. In the measured valence spectra for the SiO_2/SiC structures, photoelectrons from SiO_2 layers overlapped with those from SiC substrates. Therefore, the deconvoluted valence band spectra for SiO_2 (blue lines) were estimated by subtracting the reference SiC spectra (green lines) from the SiO_2/SiC spectra (red lines). Valence band offset at SiO_2/SiC interface corresponds to the difference in the valence band maximum between SiO_2 and SiC determined by linear extrapolation of the leading edges of the measured SiC and deconvoluted SiO_2 valence band spectra. The obtained valence band offsets at SiO_2/SiC interface with Ar-POA at 900 and 1100 °C were found to be 0.05 and 0.1 eV larger than that without Ar-POA. By taking into account the band gap of 4H-SiC (3.26 eV), we can conclude that ΔE_c at SiO_2/SiC interface was slightly decreased after Ar-POA depending on the annealing temperature.

Next, we examined the changes in the interface properties and band structures induced by Ar-POA based on electrical characterizations of SiC-MOS capacitors with 40-nm-thick SiO_2 gate dielectrics. Fig. 4(a) shows the bidirectional C–V characteristics of SiC-MOS capacitors with and without Ar-POA measured by sweeping the gate voltage from −10 V to 10 V and back to −10 V at a frequency of 1 MHz. The C–V curve for the as-oxidized sample exhibits a stretch-out shape, a small hysteresis and positive V_{FB} shift from the ideal value, suggesting the existence of large amount of interface traps and negative fixed charges. The Ar-POA at 1100 °C could effectively reduce the traps and charges, thus resulting in

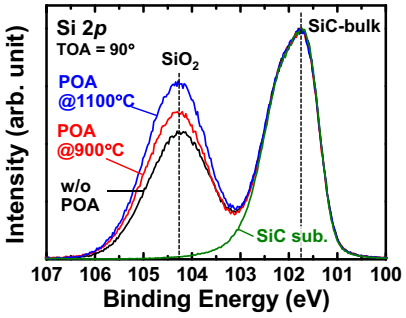

Fig. 1. Si 2*p* core-level spectra taken from 3-nm-thick SiO_2 surfaces for the samples oxidized at 1100 °C with and without Ar-POA at either 900 or 1100 °C, together with a spectrum from a bulk 4H-SiC(0001) reference. Peak intensity was normalized by bulk Si 2*p* signal.

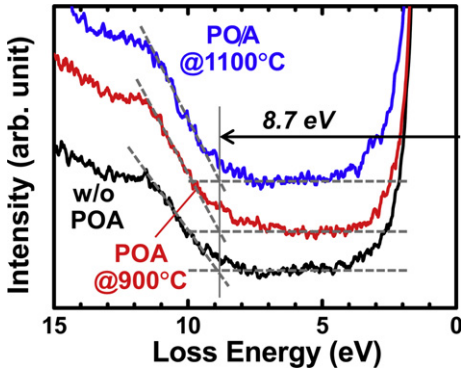

Fig. 2. O 1*s* energy loss spectra for SiO_2/4H-SiC(0001) structures with and without Ar-POA. The zero of the energy loss scale is identical to the binding energy of O 1*s* peak. The onset of the excitation from the valence to conduction bands (band gap) can be determined from the loss spectra.