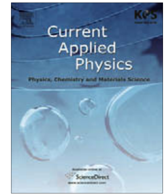
Current Applied Physics 9 (2009) 967–971

Contents lists available at ScienceDirect

Current Applied Physics

journal homepage: www.elsevier.com/locate/cap



Field emission properties of silicon field emitter arrays with volcano-shaped gate structure

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ARTICLE INFO

Article history:
Received 5 November 2007
Received in revised form 16 July 2008
Accepted 25 September 2008
Available online 14 October 2008

PACS:
85.45.Bz
85.45.Db

Keywords:
Volcano-shaped gate
Sputtering
Aging effects
F–N equation
Field enhancement factor

ABSTRACT

Field emission properties of silicon field emitter arrays (Si-FEAs) with sputtered gate structures were described and analyzed about two different tip structures surrounded by volcano-shaped gates. The resulted field emission characteristics showed that some of the emitted electrons are diverted to the gate structure because of the asymmetrical geometry of fabricated Si-FEAs with volcano-shaped gate structures. However, although the gate structures of fabricated FEAs had fragile and non-uniform edged shapes as a result of the shadow effect during sputtering and lift-off process in ultrasonic bath, it was possible to obtain stable field emission properties as a result of electrical aging effects on the edge of the non-uniform gate electrode as well as the surface of silicon tip after repeated measurements. From the Fowler–Nordheim (F–N) plots and F–N equations, it was confirmed that the field enhancement factor was abruptly changed through the electrical aging and was more influenced in case of the volcano-shaped lateral tip structure.

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1. Introduction

There has been a need for economical fabrication processes for field emitters in order to widen the applications of vacuum micro/nanoelectronics to sensors and electron sources [1,2]. There have been considerable advances in new materials, such as carbon nanotubes, nanorod, nanofiber bundles [3–5]. However, despite the demerits, such as size limitations, it is still essential to develop silicon field emitter arrays (Si-FEAs) to make all fabrication process steps compatible with integrated circuit fabrication [6,7]. In the fabrication of micro/nanosized silicon field emitter arrays, electron gun evaporation has mainly been used as a method for producing gate electrodes. This method has the advantage that fewer defects remain on the wafer after evaporation because it operates under high vacuum (approximately 10^{-6} torr). However, it requires a long process time due to the need to heat the filament [8], and it is difficult to apply this method to fabrication on a large area substrate because it uses a point source material [9]. Sputtering may be used instead of evaporation for gate electrode deposition in Si-FEA fabrication [10,11]. It operates at a relatively low pressure (approximately tens of mtorr) and it is possible to reduce the processing time. However, the sputtered gate electrode has a thin and fragile structure, particularly around the emitter tip, on account of its volcano-shape and the effect of step coverage during sputtering [10]. Therefore, the structure may have a larger resistivity than that of the evaporated gate.

In this paper, two types of volcano-shaped silicon field emitters were fabricated by sputtering as a process for fabricating a gate electrode, and their structural and electrical characteristics were examined. One structure was a sharpened Si-FEA around a volcano-shaped gate and the other was a volcano-shaped lateral Si-FEA around a volcano-shaped gate. The effect of the volcano-shaped gate structure on field emission was evaluated from a comparison and analysis of the field emission properties of the two different geometries. The results suggest that sputtering can be used to fabricate of Si-FEAs.

2. Experiments

As a result of the sputtering method, devices with a volcano-shaped gate were fabricated, as shown in Fig. 1e. However, a silicon tip may be located lower than the edge of the gate electrode in the fabricated structure because of the effect of the step coverage during gate sputtering. Therefore, the electric field at the apex of the Si tip in the volcano-shaped gate might become smaller than that in normal cases where the tip is located as high as the gate electrode [12]. As a result, it is essential to control and minimize the difference in height between the tip and gate electrode. Up to now, additional gate insulators have been used to reduce the difference in

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doi:10.1016/j.cap.2008.09.012

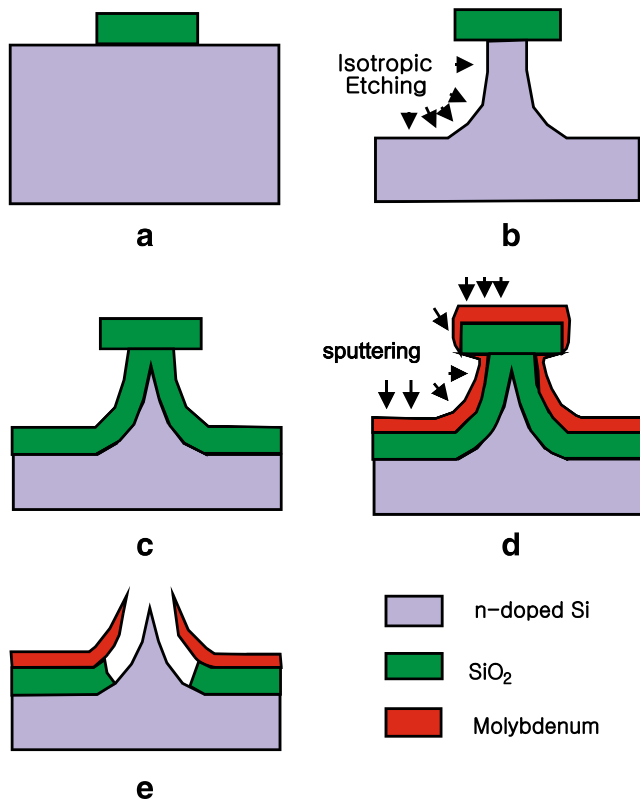

Fig. 1. Schematic diagram of fabrication process of sputtered Mo gated silicon field emitter: (a) formation of tip mask, (b) isotropic dry etch of silicon, (c) sharpening oxidation, (d) molybdenum sputtering, and (e) lift-off of overlaying structure on the tip in ultrasonic bath.

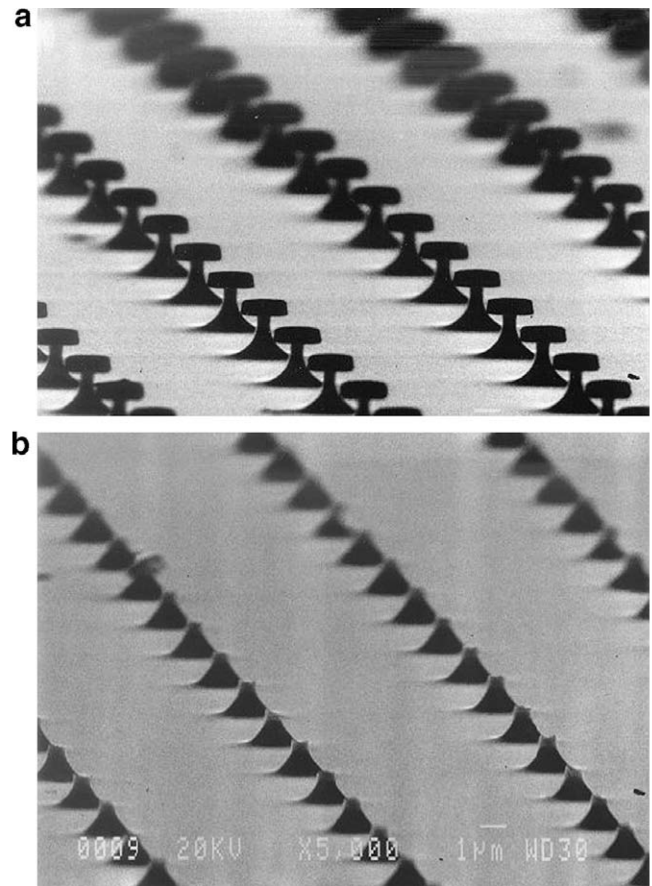

Fig. 2. Scanning electron micrographs in fabrication of silicon field emitter arrays (a) isotropic Si dry etch (b) fabricated silicon Si-FEAs.

height between the tip and gate electrode in both cases of the evaporated gate structure and the sputtered gate structure [13–15].

Without the additional gate insulator, the silicon tip was formed as high as the edge of the gate electrode by controlling the process conditions for silicon dry etching and sharpening oxidation. Silicon was etched at high RF power in order to produce a silicon tip with a high aspect ratio. The tip sharpening oxidation time was minimized in order to prevent oxidation-induced tip reduction.

Fig. 1 shows the fabrication process. A SiO_2 layer as thick as 5500 Å was deposited by PECVD on a phosphorus doped n-type silicon wafer and patterned into a disk with a diameter of 1.4 μm and 1.6 μm by conventional photolithography, as shown in Fig. 1a. The silicon was then etched isotropically by 1.5 μm, as shown in Fig. 1b. A silicon etch was performed under the following conditions: RF power of 350 W, 25 sccm SF_6, and a pressure of 250 mtorr. The aspect ratio defined as the ratio of vertical etching to lateral etching was 2.72. Fig. 2a shows the scanning electron micrograph of the etched Si-FEAs. Wet oxidation was then performed for 70 min at 950 Å to make the emitters sharp, as shown in Fig. 1c, and a thermal oxide with a thickness of 3700 Å was obtained. However, the apex of the tip was not sharpened in case of a 1.6 μm diameter because of the inadequate oxidation time. Therefore, a volcano-shaped silicon tip was obtained as a result of insufficient oxidation, and the resulting silicon tip was as high as the volcano-shaped gate.

A 1500 Å thick molybdenum layer was deposited by RF sputtering at a pressure of 5×10^{-2} torr at a power of 1.5 kW. As a result of the shadowing effect, the thickness of the molybdenum layer at the bottom of the disk was relatively thin, as shown in Fig. 1d. Therefore, the oxide disks were not easily stripped away in the buffered HF solution due to the presence of sputtered molybdenum on the bottom of the disks. Accordingly, oxide disks were removed physically and etched chemically in a buffered HF solution for 10–15 min in an ultrasonic bath, which exposed the silicon emitters.

3. Results and discussion

Fig. 2b shows the scanning electron micrograph of the fabricated Si-FEAs and the arrays with a volcano-shaped gate structure. Fig. 2b does not show the silicon tips in the gate structures. Fig. 3a and b shows the cross-sectional views of fabricated emitters for the sharpened silicon tip in the volcano-shaped gate and for the volcano-shaped lateral silicon tip in the volcano-shaped gate, respectively. Fig. 3a and b shows that the structure of the gate electrode is thin and unstable as a result of sputtering and lift-off caused by the ultrasonic wave in the ultrasonic bath. The diameter of the volcano-shaped gate shown in Fig. 3a was approximately 0.4 μm, and the sharpened silicon tip was 1.26 μm in height with an aspect ratio of 1.66:1 (vertical–horizontal). As a result of silicon etching with a RF power of 350 W, the silicon tip was located slightly lower than the edge of the gate electrode. However, it is difficult to define the distance between the tip and the edge of the gate electrode because the array contains unstable gate structures, as shown in the rear region of Fig. 3a. In the case of Fig 3b, it is more difficult to define the distance between the lateral tip and the gate electrode.

From Fig. 3a and b, the oxide layer between the volcano-shaped gate and the silicon tip was removed very deeply because the thermal oxide had been wet etched for 10–15 min after removing the oxide disk. A long time is needed for the lift-off process because all the oxide masks should be removed for the 625 tip arrays.

The FEAs consisting of 625 tips were characterized electrically in a vacuum environment of 1×10^{-8} torr. Two Keithley 6487

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