

## Effect of poly silicon thickness on the formation of Ni-FUSI gate by using atomic layer deposited nickel film

Jong-Bong Ha, Sang-Won Yun, Jung-Hee Lee \*

School of Electrical Engineering and Computer Science, Kyungpook National University, 1370 Sankyuk-dong, Buk-gu, Daegu 702-701, Republic of Korea

### ARTICLE INFO

#### Article history:

Received 6 August 2008  
Received in revised form 16 February 2009  
Accepted 21 April 2009  
Available online 3 May 2009

#### PACS:

73.40.Qv  
73.40.Q

#### Keywords:

Metal gate  
Nickel silicide phase  
Atomic layer deposition  
Fully silicidation  
Flatband voltage

### ABSTRACT

The effect of poly-Si thickness on silicidation of Ni film was investigated by using X-ray diffraction, auger electron spectroscopy, cross-sectional scanning transmission electron microscopy, resistivity,  $I$ - $V$ , and  $C$ - $V$  measurements. The poly-Si films with various thickness of 30–200 nm were deposited by LPCVD on thermally grown 50 nm thick  $\text{SiO}_2$ , followed by deposition of Ni film right after removing the native oxide. The Ni film was prepared by using atomic layer deposition with a  $\text{N}^2$ -hydroxyhexafluoroisopropyl- $\text{N}^1$  (Bis-Ni) precursor. Rapid thermal process was then applied for a formation of fully silicide (FUSI) gate at temperature of 500 °C in  $\text{N}_2$  ambient during 30 s. The resultant phase of Ni-silicide was strongly dependent on the thickness of poly-Si layer, continuously changing its phase from Ni-rich ( $\text{Ni}_3\text{Si}_2$ ) to Si-rich ( $\text{NiSi}_2$ ) with increasing the thickness of the poly-Si layer, which is believed to be responsible for the observed flat band voltage shift,  $\Delta V_{\text{FB}}$ , in  $C$ - $V$  curves.

© 2009 Elsevier B.V. All rights reserved.

### 1. Introduction

Metal gates have been suggested to replace the conventional poly-Si gate which suffers from poly depletion and boron penetration. Recently, various silicides have attracted much more attention as promising candidates for the metal gates because they are compatible with traditional CMOS process and exhibit a possibility of tunable work function [1,2]. Due to its high line width independent conductivity, the relatively small amount of Si consumption during its formation, and its low formation temperature, Ni fully silicided (Ni-FUSI) gate has become an alternative to the titanium and cobalt silicides, currently used Si device technology, and even further beyond the 65 nm technology node [3–5]. However, the success of its integration is strongly related to the phase control which significantly varies the effective work function of the material. A higher work function, attractive for pMOSFET devices [6,7] can be easily obtained with Ni-rich silicides, such as  $\text{Ni}_2\text{Si}$ ,  $\text{Ni}_3\text{Si}_{12}$ , or  $\text{Ni}_3\text{Si}$ . The NiSi phase which has the lowest resistivity among various phases is found to have mid-gap work function. On the other hand, obtaining a different phase of Ni-silicide which should have a lower work function attractive for nMOSFET devices still remains

questionable. Wen et al. showed that the phase of Ni-silicide and, correspondingly, the flat band voltage shift could be controlled with the thickness of Ni film. Analogously, the investigation on the poly-Si thickness dependency is also important for the phase-controlled FUSI process. Kittl et al. demonstrated the Ni-FUSI gate with dual work function can be integrated by using different poly-Si thickness for nMOSFET and pMOSFET [8]. The optimization of polycrystalline Si according to the deposition temperature was also reported for 45 nm node Ni-FUSI [9,10].

In this work, we present for the first time a detailed study on the poly-Si thickness dependent phase formation for Ni-FUSI converted from Ni film deposited by atomic layer deposition (ALD). The device size is scaling-down and CMOS structure is also changing from planar type to 3-D type such as emerging FinFET, which needs better step coverage, uniformity, and cleanness in the deposited film. The Ni deposition with ALD is, therefore, a very promising for obtaining high quality Ni-silicide because it has superior uniformity and step coverage as well as cleanness compared to other deposition methods. In addition, the process temperature for ALD is relatively low compared to conventional CVD methods, which is also very attractive in nano-scale CMOS technology [11,12], and also examine the possible application of Ni-FUSI as a tunable work function gate electrode, especially for a lower work function.

\* Corresponding author. Tel.: +82 53 940 8655; fax: +82 53 950 7932.  
E-mail address: [jlee@ee.knu.ac.kr](mailto:jlee@ee.knu.ac.kr) (J.-H. Lee).

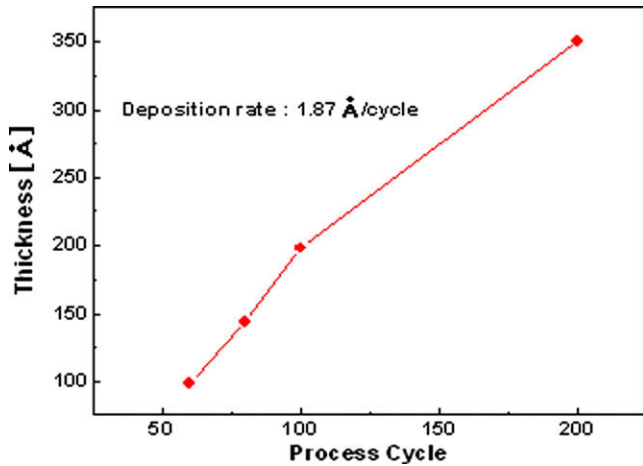


Fig. 1. The Ni deposition thickness as a function of the cycle number at 220 °C.

## 2. Experiments

Ni-FUSI capacitors were fabricated on (1 0 0) p-type Si wafers with a resistivity of 9–12 Ω cm. First, 50 nm-thick SiO<sub>2</sub> film was thermally grown at 950 °C. Poly-Si films with different thicknesses (30, 40, 75, 100, 150, and 200 nm) were subsequently deposited by LPCVD at 625 °C and capacitor patterns were then defined. The radius of top electrode on circular capacitor is 200 μm. After removal of the native oxide on poly-Si, 35 nm-thick Ni film was deposited by ALD at 220 °C. According to the theoretical ratio of the amount of Ni reacting with Si to form NiSi (Ni:Si:NiSi = 1:1.84:2.22) [8,9], the poly-Si thickness of 65 nm is assumed to be the threshold thickness for FUSI of a 35 nm Ni film. For the ALD, Bis-Ni was used as a metal organic precursor, H<sub>2</sub> as the reactant gas, and Ar as the purging gas. The thickness of the deposited Ni film is almost linearly dependent on the number of deposition cycles with a deposition rate of about 1.87Å/cycle, as shown in Fig. 1 [13]. Rapid thermal processing (RTP) was then performed at 500 °C in N<sub>2</sub> ambient during 30 s to form Ni-silicide, followed by removal of un-reacted Ni using HCl:FeCl<sub>3</sub>:HNO<sub>3</sub>:H<sub>2</sub>O solution.

Fig. 2 shows the schematic process flow for the Ni-FUSI gates with various poly-Si thicknesses. Material analysis for phase and morphology characterization includes X-ray diffraction (XRD), auger electron spectroscopy (AES), and scanning transmission electron microscopy (STEM). The resistances of films were measured

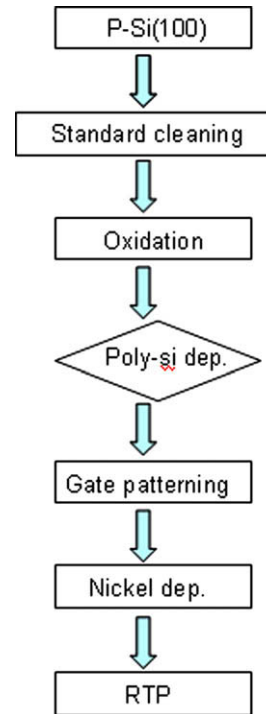


Fig. 2. The schematic process flow for the Ni-FUSI gates with various poly-Si thicknesses.

by four-point probe and *I*–*V* and *C*–*V* characteristics were analyzed by HP4156 and HP4280, respectively.

## 3. Results and discussion

As shown in Fig. 3, the phases of Ni-silicide were observed by XRD for samples formed on poly-Si layers with various thicknesses. Any peaks related to the phase of Ni-silicide were not observed for the sample converted from the 30 nm-thick poly-Si. This is because Ni was converted to Ni-rich silicide film with high Ni composition after RTP due to insufficient amount of Si atoms in 30 nm-thick poly-Si layer to react with 35 nm-thick Ni layer and thus the Ni-rich film was easily removed during etching the residual Ni layer on the film. Formation of a weak Ni-rich phase (Ni<sub>3</sub>Si<sub>2</sub>) was

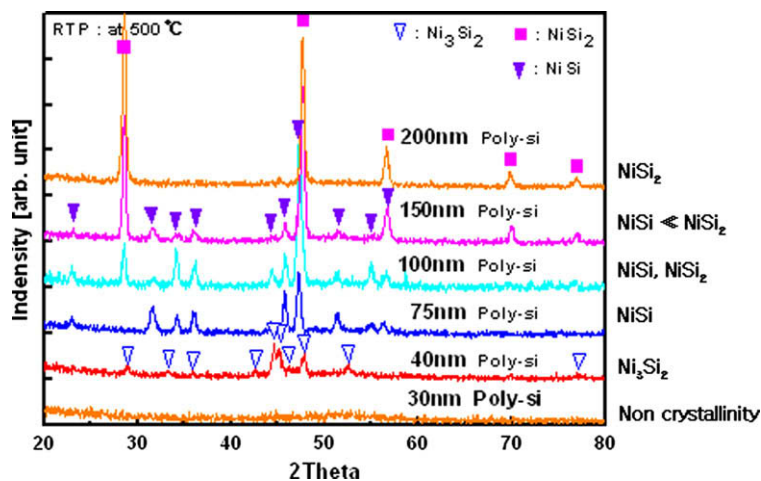


Fig. 3. X-ray diffraction spectroscopy of fully silicide gates as a function of poly-Si thickness.

Download English Version:

<https://daneshyari.com/en/article/1788873>

Download Persian Version:

<https://daneshyari.com/article/1788873>

[Daneshyari.com](https://daneshyari.com)