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Modeling of transient and steady-state dark current in amorphous silicon *p–i–n* photodiodes

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ABSTRACT

A theoretical model for describing the bias-dependent transient and steady-state behavior of dark current in hydrogenated amorphous silicon (*a*-Si:H) *p–i–n* photodiode has been developed. An analytical expression for the bias-dependent steady-state thermal generation current is derived by solving the continuity equations for both electrons and holes. The model for describing transient dark current in *a*-Si:H *p–i–n* photodiode is developed by considering the depletion of electrons from the *i*-layer and carrier injection through *p–i* interface. For photodiodes that have very good junction properties, the high initial dark current decreases with time monotonously and reaches a plateau. However, in case of poor junctions, the injection current can be the dominating mechanism for transient leakage current at relatively high biases, the dark current decays initially and then rises to a steady-state value. The proposed physics-based dark current model is compared with published experimental results on several photodiodes. The comparison of the model with the experimental data allows an estimate of active dopant concentration in the *p*-layer and the defect density in the midgap of *i*-layer.

1. Introduction

Hydrogenated amorphous silicon (*a*-Si:H) *p–i–n* photodiodes are increasingly being used in large-area indirect conversion medical imaging sensors and solar cells [1,2]. The reverse-bias dark current in these applications is a sensitive measure of their device performance. In a typical *a*-Si:H *p–i–n* detector structure, the thickness of the *i*-layer is ~1 μm whereas the thickness of the *p*- or *n*-layer is ~50 nm [3]. The possible sources of dark current in *a*-Si:H *p–i–n* photodiodes are the bulk thermal generation in the *i*-layer, emission of carriers from the *p–i* and *i–n* interfaces, contact injection, and edge leakage [4,5]. Since edge leakage is proportional to device perimeter, edge leakage tends to be least significant in large-area devices [4]. It has been found that, for *p–i–n* detector structures that provide good blocking contact layers, the contact injection currents are negligible because of almost zero electric field at the contacts.

Several theoretical models have been proposed to describe the leakage currents of *a*-Si:H *p–i–n* detectors [4], [6–8]. Street derived an analytical expression for the steady-state thermal generation current [4]. The steady-state thermal generation model given by Street has no voltage dependency. In practice, there is a significant voltage dependency of the steady-state thermal generation current at low biases [9]. The one-dimensional steady-state carrier transport in *a*-Si:H *p–i–n* detector structures under reverse-bias has been studied by using amorphous semiconductor device modeling program (ASDMP) [6,8]. All these analyses are concentrated on the steady-state reverse-bias dark current. Kim and Cho [7] investigated the transient dark current behavior in *p–i–n* diodes by combining Street's model for thermal generation current with the interface injection current. However, it overestimated the injection current at low biases. In this work, we have proposed an explicit analytical expression for the transient dark current due to depletion of electrons from the *i*-layer, and for the injection current through the *p–i* interface by considering energy band bending at the interface and Poole–Frenkel barrier lowering effect. We have also developed an analytical expression for the steady-state ther-

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mal generation current by solving the continuity equations for both electrons and holes. The time and voltage dependent total dark current is obtained by adding the thermal generation current with the injection current through the *p–i* interface. The dark current model is compared with the published experimental data on several photodiodes. The comparison of the model with the experimental data allows an estimate of active dopant concentration in the *p*-layer and the defect density in the midgap of *i*-layer.

2. Analytical model

The *i*-layer is slightly *n*-type and thus the Fermi level E_F at zero bias is above the midgap. After applying the bias, electrons are depleted from the *i*-layer and the steady-state quasi-Fermi level E_{FD} lies below E_F. Fig. 1 shows the energy band diagram near *p–i* interface at steady-state. The quasi-Fermi level E_{FD} bends near the interface to align with the Fermi level of the *p*-layer. The amount of band bending $\Delta\phi$ within the *p*-layer near *p–i* interface due to the applied voltage can be determined by solving the Poisson's equation. Note that the doping concentration near the interface can be somewhat lower than the bulk value in some structures, which creates an additional bending of the conduction band at the interface [3]. The width of the depletion layer in the *p*-region depends on the doping concentration of the *p*-layer [9]. Assuming full depletion of *i*-layer at high voltage and a constant quasi-Fermi level in the *p*-layer, and solving Poisson's equation at the *p–i* interface, $\Delta\phi = (\varepsilon_s/2N_a)F_1^2$, where N_a is the active dopant concentration in the *p*-layer, $\varepsilon_s(=\varepsilon_0\varepsilon_r)$ is the permittivity of the amorphous silicon and F_1 is the electric field at the *p–i* interface. Assuming built-in voltage, $V_{bi} \sim 1.2$ V [10] and the *i*-layer thickness of 1 μm, the built-in electric field in the *i*-layer is $\sim 10^4$ V/cm, whereas the typical applied field is $\sim 10^5$ V/cm. The quasi-Fermi level is a function of position within a small region of thickness x_1 in the *i*-layer near *p–i* interface. The thickness, $x_1 \approx [kT\ln(N_a/n_i) - \Delta\phi]/eF_1$ where, k is the Boltzman constant, T is the absolute temperature, and n_i is the intrinsic carrier concentration in the *i*-layer. Assuming $N_a = 2 \times 10^{18}$ cm^{-3}, $n_i \sim 10^8$ cm^{-3} [11], and $F_1 = 10^5$ V/cm, the estimated values of $\Delta\phi = 0.016$ eV and $x_1 \sim 60$ nm. Therefore, for a typical device length of about 1 μm it is reasonable to assume a constant difference between the Fermi level and the conduction band throughout the *i*-layer. The initial decay in thermal generation current of *a*-Si:H detector can be explained by depletion of electrons from the *i*-layer. The temporal behavior of the carrier depletion process is determined by the detrapping time constants. Therefore, the transient current due to electron depletion can be expressed as [12],

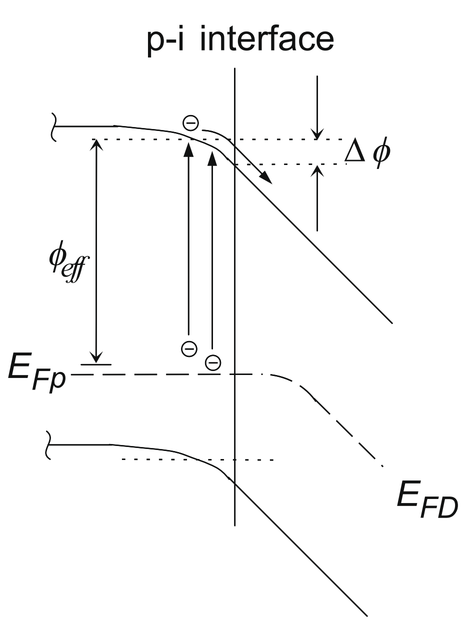

Fig. 1. Schematic energy band diagram at the *p–i* interface.

$$J_{dep}(t) = \frac{eL}{2}\int_0^{E_c} \frac{N(E)}{\tau_d(E)}\left\{\frac{1}{1+\exp[(E-E_F)/kT]} - \frac{1}{1+\exp[(E-E_{FD})/kT]}\right\}\exp\left[-\frac{t}{\tau_d(E)}\right]dE, \quad (1)$$

with a mean detrapping time constant,

$$\tau_d(E) = \omega_0^{-1}\exp[(E_C - E - \beta_{pf}\sqrt{F_0})/kT], \quad (2)$$

where $N(E)$ is the density of states of *a*-Si:H at energy E in the midgap, E_C is the conduction band edge, F_0 (=V/L) is the applied field, V is the bias voltage, L is the intrinsic layer thickness, ω_0 is the attempt-to-escape frequency, and $\beta_{pf} = \sqrt{e^3/\pi\varepsilon}$ is the Poole–Frenkel coefficient. Assuming uniform carrier depletion throughout the *i*-layer, the electric fields at the *p–i* and *n–i* interfaces can be written as,

$$F_1(t) = F_0 + \frac{eLn_d(t)}{2\varepsilon_s}, \quad (3)$$

and

$$F_2(t) = F_0 - \frac{eLn_d(t)}{2\varepsilon_s}, \quad (4)$$

where $n_d(t)$ is the time-dependent depleted electron concentration in the *i*-layer, F_1 and F_2 are the electric fields at the *p–i* and *n–i* interfaces, respectively.

In *p–i–n* structure, besides thermal generation in the *i*-layer, electron injection through *p–i* interface is a possible source of current at higher fields. Hole injection through *n–i* interface is negligible because of the lower electric field at the *n–i* interface [13] (this is also evident from Eqs. (3) and (4)) and the low hole mobility. The *p–i* interface is a high field region, contains a high defect density and thus, at room temperature, interface field enhanced generation can be the dominating process at higher applied fields [9]. The carriers are injected from the distributed trap states near E_{Fp} at the *p–i* interface as shown in Fig. 1. We can define an effective barrier height ϕ_{eff} for the injected electrons. The band bending $\Delta\phi$, defined previously, lowers the physical barrier at the interface in addition to Poole–Frenkel barrier lowering effect. Once the carriers are injected into the intrinsic layer, they move by drift mechanism (diffusion component of current is negligible compared its drift component because of very high applied voltage) [14,15].Therefore, the reverse current density in low mobility (effective drift mobility, $\mu < 1$ cm^2/V–s) semiconductor due to electron injection through *p–i* interface can be written as [14,15],

$$J_{inj}(t) = e\mu_e N_C F_1(t)\exp\left\{-\frac{\phi_{eff} - \beta_{pf}\sqrt{F_1(t)} - \Delta\phi}{kT}\right\} \cong e\mu_e n_{inj}F_1(t), \quad (5)$$

where μ_e is the drift mobility of electrons, N_C is the effective density of states in the conduction band, and n_{inj} is the average injected carrier concentration through *p–i* interface.

The steady-state thermal generation current in *a*-Si:H detectors arises from the carriers excited from the deep states near E_{FD} to the band edges of the intrinsic layer. The perturbation of applied electric field in the *i*-layer due to the space charge is usually very small. The electric field at the *p–i* interface is usually $1.1 \sim 1.3$ times higher than that at the *n–i* interface, the thermally generated carriers will move with a slightly higher velocity near *p–i* interface compared to that near *n–i* interface. Therefore, assuming a