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Fabricating high performance n-channel lateral double diffused metal–oxide–semiconductor transistors utilizing the shallow trench isolation as a salicide blocking mask of the drift region

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Abstract

In this paper, the improved characteristics of 10 V tolerant high-voltage n-channel lateral double diffused metal–oxide–semiconductor (LDMOS) devices, using a pure 0.25 μm standard low-voltage complementary metal–oxide–semiconductor (CMOS) logic process with dual gate oxide, are described. The fabricated transistors showed about 30% better current driving characteristics and about 40% higher drain operating voltage than previous reports of these kinds of devices. The transistors maintained a breakdown voltage, BV_{DSS}, over 14 V. These devices also showed good sub-threshold characteristics. This paper describes the cost-effective and high performance n-channel high-voltage LDMOS using a pure low-voltage standard CMOS logic process.

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1. Introduction

Embedding high-voltage MOS devices into the standard low-voltage logic process has been one of the most important goals of developing a cost-effective system on a chip (SoC) solution in fields of display driver, non-volatile memory driver and high frequency power amplifier circuitry [1–4]. Holland and Igic developed a dedicated process flow to implement high-voltage MOS devices into the standard low-voltage logic process. This device has high breakdown voltage exceeding 100 V, but processing cost is high. Recently, high-voltage lateral double diffused metal–oxide–semiconductor (LDMOS) transistors have been embedded into the submicron low-voltage standard complementary metal–oxide–semiconductor (CMOS) logic process while maintaining base line process sequence [5–7]. Letavic et al. suggested the LDMOS with field oxide inside the unit cell using a 0.25 μm standard CMOS process. In this paper, additional two photo masks and high energy ion implantation steps were included in a 0.25 μm standard CMOS process. Additional photo masks and implantation steps provided performance improvements of the fabricated devices. Mitros et al. reported on these embedded LDMOS devices that used a 0.18 μm CMOS process flow with well ion implantation adjustment. This device structure, however, was not suitable for the submicron standard CMOS process. This device needed a self-aligned silicide (salicide) protection layer in the drift region. This structural issue will be discussed more in detail in the following paragraphs. Ramos et al. also reported on a new embedded LDMOS device using the 0.35 μm standard CMOS process. This device used floating polysilicon as

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the n+ implantation masking layer to form a lightly doped extended drain region. For these new LDMOS device structures, however, coupling effect and channel-hot-carrier reliability that originated from the floating polysilicon on drift region were not considered. In the previous reports of these LDMOS devices, the device structure and/or geometries – e.g. channel length, drift length – were not optimized. Therefore, the maximum drain operation voltage, $V_{DS,MAX}$, of the n-channel LDMOS transistors was limited to the range between 7 and 8 V. Also, the current driving characteristics, $I_{D,SAT}$, were about half of those of the standard low-voltage CMOS logic transistors. The $I_{D,SAT}$ and $V_{DS,MAX}$ of previous LDMOS devices need to be improved. This is because applications of high-voltage LDMOS devices are limited by the $V_{DS,MAX}$. By increasing this $V_{DS,MAX,}$ these transistors can then be used in various circuit applications. Also, improvement in the $I_{D,SAT}$ can reduce the silicon die area.

In this paper, we report on the fabrication of high-voltage n-channel LDMOS devices, using a 0.25 μm pure standard CMOS logic process, without any process modification. Our fabricated devices showed higher current driving and improved drain operating voltage characteristics than those devices described in previous reports.

2. Device structure and fabrication

The cross-section of the fabricated LDMOS device is shown in Fig. 1. A lightly doped n-well layer can play the role of a drift region which reduces the drain electric field. Therefore, with this layer, the drain breakdown voltage can be increased. This device structure has an advantage of embedding into the submicron low-voltage CMOS logic process as design rule scales down. For the standard CMOS logic process at 0.25 μm and below, source and drain contact regions need a salicide layer – e.g. $TiSi_2$ or $CoSi_2$ –to reduce the contact resistance by a small contact opening area. However, to ensure higher $V_{DS,MAX}$ for LDMOS devices, without shallow trench isolation (STI) field oxide on the drift region, an additional salicide blocking layer must be inserted on the drift region. These salicide blocking layers need an extra space from other adjacent layers. For our fabricated devices, the STI field oxide on the drift region acts as a salicide masking layer. Consequently, a self-aligned salicide layer was formed by the STI field oxide on the drift region.

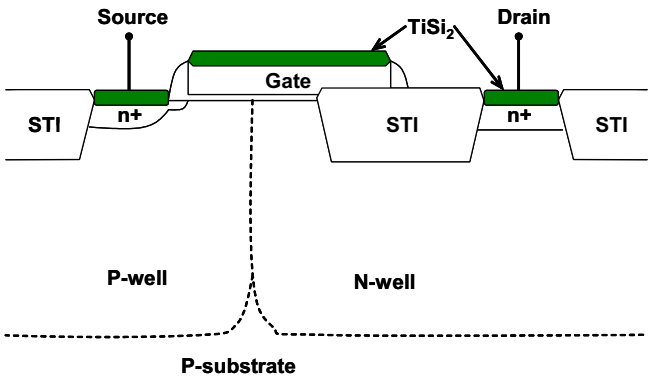

Fig. 1. Cross-section of the fabricated LDMOS devices.

A 0.25 μm low-voltage standard CMOS logic process with 2.5 and 3.3 V dual gate oxide was used to fabricate these LDMOS devices. The process flows for the LDMOS devices are as follows. First, the STI was formed on the p-type (1 0 0) silicon wafer. The n-well and the p-well regions were formed, sequentially, by ion implantation. No additional threshold voltage (V_T) adjust implantation was performed. Then, dual gate oxidation and gate formation were accomplished. The electrical gate oxide thicknesses of the fabricated LDMOS devices were 5.2 and 7.1 nm, respectively. Then n-lightly doped drain (LDD) oxide sidewalls and n+ and p+ source drain junctions were formed. Next, $TiSi_2$, polysilicon-to-metal (PMD) dielectrics, contacts, and the metal interconnection steps were accomplished.

3. Experimental results

Fig. 2a shows the drain current versus the drain voltage characteristics for the two gate oxide devices ($T_{OX} = 5.2$ and 7.1 nm). The design parameters and measurement conditions of the devices are annotated in this figure. The measured drain breakdown voltage was about 14.25 V. The drain current slope (g_{ds}), in the saturation region, was small, that is up to 10 V. In this figure, the drain operation voltage can be extended up to 10 V for both the 5.2 and 7.1 nm gate oxide devices.

Fig. 2b shows the drain current versus gate voltage characteristics for the two gate oxide devices. The measured linear extrapolated threshold voltages were 0.58 and 0.84 V for the 5.2 and 7.1 nm gate oxide devices, respectively. Measured threshold voltages of the devices strongly depended on the thickness of the gate oxides. No significant leakage currents or abnormal current hump effects were monitored in the sub-threshold regime. The curves of the 10 V drain voltage showed no sign of punch-through. Small threshold voltage shifts were found between the triode and the saturation regimes.

Fig. 3 shows the $I_{D,SAT}$ and the BV_{DSS} versus the effective channel length for the two gate oxide devices. The measured BV_{DSS} was over 14 V throughout the variation of the effective channel length ($L_{eff.}$) from 0.5 to 1.5 μm. The saturation drain currents increased as the effective channel lengths decreased while maintaining a BV_{DSS} of about 14 V. Measured drain saturation currents of the fabricated devices at $L_{eff.}$ of 0.5 μm were 426 and 456 μA/μm for the 5.2 and 7.1 nm devices, respectively. Consequently, current driving characteristics and the drain operation voltage improved from those of previous reports [6,7]. In addition, the saturation drain currents of the 7.1 nm gate oxide devices were slightly higher than those of the 5.2 nm gate oxide devices, because the overdrive voltage ($V_{eff.} = V_{GS} - V_T$) of the 7.1 nm gate oxide transistors was higher