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Catalyst-free growth of InP nanowires on patterned Si (001) substrate by using GaAs buffer layer

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ABSTRACT

The catalyst-free metal organic vapor phase epitaxial growth of InP nanowires on silicon (001) substrate is investigated using selectively grown GaAs buffer layers in V-shaped trenches. A yield up to 70% of nanowires is self-aligned in uncommon ⟨112⟩ directions under the optimized growth conditions. The evolution mechanism of self-aligned ⟨112⟩ directions for nanowires is discussed and demonstrated. Using this growth method, we can achieve branched and direction switched InP nanowires by varying the V/III ratio in situ. The structure of the nanowires is characterized by scanning electron microscope and transmission electron microscopy measurements. The crystal structure of the InP nanowires is stacking-faults-free wurtzite with its c axis perpendicular to the nanowire axis.

1. Introduction

Integrated III–V nanowires on Si have been praised for combining all of the advantages of III–V semiconductors, such as direct band-gap, high carrier mobility, and advanced band-structure engineering with silicon microelectronics technology [1–3]. Furthermore, Indium Phosphide (InP) is a key building block in III–V heterojunction devices which is widely used in optical communications and high speed integrated circuits. In most cases, heteroepitaxial growth of InP nanowires on Si has been performed by using gold particles as a catalyst in the so-called vapor liquid–solid (VLS) mechanism [4–6]. However, gold is a forbidden element in CMOS processing, as it forms mid-gap electronic states in Si [7], which has a very high solid diffusivity, and it is extremely hard to be removed from the exposed fabrication equipment. Recently, catalyst-free (or self-catalyzed) growth of InP nanowires using in situ deposited In droplets as seeds on Si substrate was reported [8,9]. Nevertheless, there is a need for a more controllable growth scheme for Si (001) substrate. The use of Si (001) oriented substrates is preferable, considering its potential compatibility with processing in standard microelectronics fabrication. In addition, III–V semiconductors when grown in the ⟨111⟩ B direction often exhibit a high density of stacking faults that can degrade device optical and electrical characteristics. Therefore, the growth of nanowires in other directions (which generally result in defect-free nanowires) is of great interest.

In this work, we introduce a novel means to nucleate and grow Au-catalyst-free InP nanowires on Si (001) substrate without pre-deposited In droplets. In this manner, the use of a separate step to apply the nano-catalyst to the surface is avoided. A high quality GaAs buffer layer with two convex {111} B facets was selectively grown in V-shaped trenches to promote the growth of highly uniform, direction control, single-crystal InP nanowires on Si (001) substrates. In addition, by varying the V/III mole ratio in nanowires growth process, we achieved branched and direction switched InP nanowires. This method can also be used in GaAs and InAs nanowires growth but is not in the scope of this letter.

2. Experiment

The epitaxy was performed by MOCVD (AIXTRON 200) at a pressure 50 mbar. Triethylgallium (TEGa), trimethylgallium (TMGa) and arsine (AsH_3) were used as precursors of GaAs buffer layers. InP nanowires precursors were trimethylindium (TMIn) and phosphorane (PH_3). Substrates used for InP nanowires growth were Si (001) substrates patterned with high aspect ratio V-shaped trenches along ⟨110⟩ direction and fabrication processes for substrates were reported elsewhere [10]. Growth of the InP nanowires on Si substrate was carried out as the following steps. (1) Prior to growth, thermal cleaning in an H_2 ambient was carried out at 720 °C to remove the native oxide. While wafers were being cooled from the H_2 baking temperature, AsH_3 is introduced into the reactor to form one monolayer of As-terminated Si {111} surfaces. (2) GaAs buffer layers were grown by a two-step growth

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method: the low-temperature (400 °C) nucleation layer and high-temperature (630 °C) top layer. (3) After ramped down to the desired temperature, the InP nanowires were deposited by feeding PH_3 and TMIn simultaneously. InP nanowires growth was terminated by switching off In supply while maintaining PH_3 supply until the substrate was cooled down below 250 °C. The gas-flow and temperature sequence was shown in Fig. 1. Different growth conditions were used in step 3, including growth temperature (range from 380 °C to 450 °C) and V/III ratio (range from 250 to 668). The morphologies of InP nanowires were investigated by a scanning electron microscopy (SEM). The crystal structure of the nanowires was characterized by FEI Tecnai F20 transmission electron microscopes (TEM) operated at 200 kV. For high-resolution TEM (HR-TEM) analysis, nanowires were removed from the growth substrate via sonication in ethanol and then drop-cast onto holey carbon grids.

3. Results and discussion

A top-view SEM image of InP nanowires deposited on patterned Si (001) is shown in Fig. 2(a). The process conditions were 450 °C and a V/III ratio of 250. In this SEM image, most of the nanowires appear as white lines parallel with each other and perpendicular with trenches direction. Fig. 2(b) is a side-view SEM image obtained from [1 – 10] direction, the nanowires appear vertical to the substrate. Comparing Fig. 2(a) with (b) shows that InP nanowires lie in (1 – 10) plane. In Fig. 2(c) which is obtained in [110] direction, we can see InP nanowires with two preferential growth directions, both angled 55° from the (001) plane and angled 70° from each other. As mentioned before, the nanowires lie in (1 – 10) plane, we can conclude that the nanowires elongate along the ⟨1 – 12⟩ directions. The lower-left inset shows a magnified detail of Fig. 2(c). As we previously reported, the GaAs buffer layer grown in V-shaped trenches of Si substrates has two convex {111} B surfaces [11]. In this inset, InP nanowire started from the bottom consists by GaAs and SiO2 sidewall, and grew along the GaAs {111} facets and extends to few micrometers length. From the sample shown in Fig. 2(a), about 73% nanowires are aligned in ⟨1 – 12⟩ directions.

As for the growth direction, InP nanowires preferentially grow in the ⟨111⟩ direction by MOVPE, thus many reported about nanowires growth on Si (111) substrates [12]. When the InP nanowires growth on Si (001) substrate, the angles between the nanowires and the Si substrate are diverse [13]. In this study, we report that the InP nanowires growth direction can be controlled and favor to grow in ⟨1 – 12⟩ directions. We explained growth mechanism of ⟨1 – 12⟩ favor growth directions by two growth mechanisms: misfit dislocations and mass surface diffusion, as shown schematically in Fig. 3. In the part (a), since there exists a 4.2% difference in the lattice parameters between GaAs (aGaAs = 0.565 nm) and InP (aInP = 0.587 nm), there will be many {111} type microtwins and stacking faults parallel to the InP/GaAs interface when InP nucleate on GaAs buffer layers (labeled by a dot line in InP nanowires) [14]. These twins/stacking faults can relieve

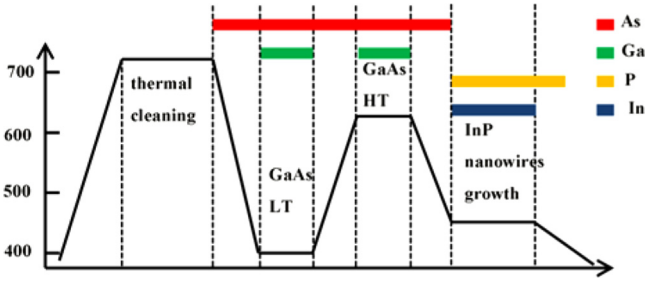

Fig. 1. Schematic illustrations of gas-flow and temperature sequence for InP nanowires growth on Si.

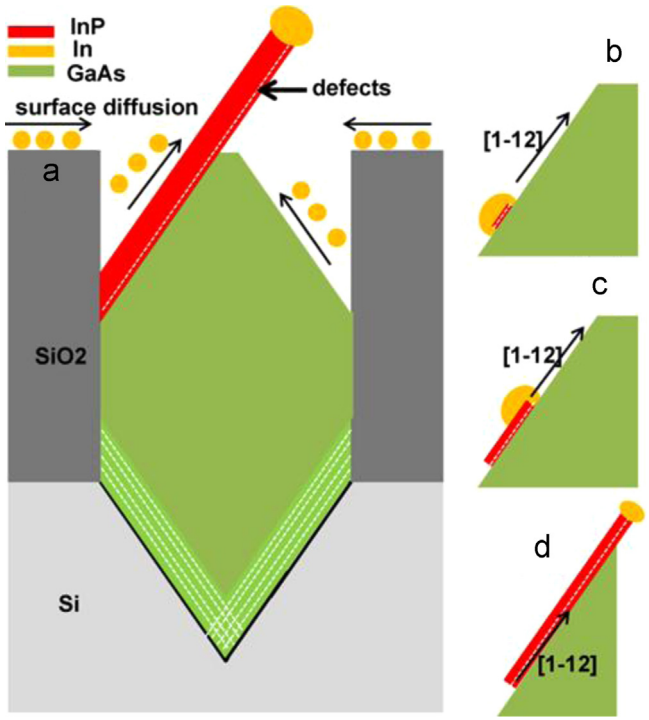

Fig. 3. Schematic diagram of the MOCVD growth mechanisms for InP nanowires on Si substrate patterned with V-shaped trenches by using GaAs buffer layer.

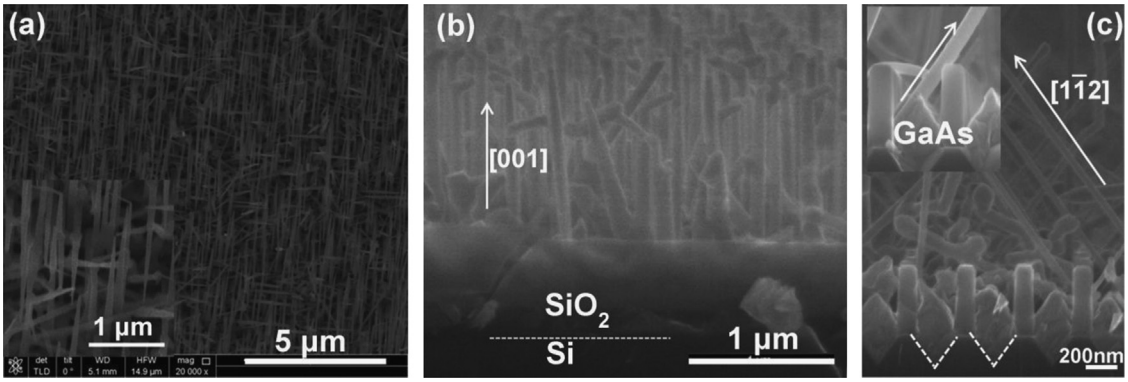

Fig. 2. SEM images of InP nanowires growth on patterned Si (001) substrates using GaAs buffer layers. (a) The top view SEM images of InP nanowires (b) A side view SEM image taken on [1 – 10] direction. (c) A typical SEM image (side view) taken on [110] direction.