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Origins of hillock defects on GaN templates grown on Si(111)

Y. Han [a,*], D. Zhu [a,b], T. Zhu [a], C.J. Humphreys [a], D.J. Wallis [a,b]

[a] Department of Materials Science and Metallurgy, University of Cambridge, 27 Charles Babbage Road, Cambridge CB3 0FS, UK
[b] Plessey Semiconductors, Tamerton Road, Plymouth, Devon PL6 7BQ, UK

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ABSTRACT

The origin of surface hillocks (also known as pancake defects) on GaN-on-Si wafers grown by MOVPE has been investigated. FIB/TEM observations confirmed that the appearance of the hillocks is due to the formation of Ga-rich precipitates within the AlGaN buffer layer. XRD (002) FWHM measurements also show that the surface hillocks are associated with a high degree of crystal tilt in the AlN nucleation layer. Two factors are considered to be the cause of such a phase separation: (1) a high density of surface steps associated with the regions of large crystal tilt which act as nucleation centers and (2) a lower mobility of Al adatoms at the growth surface compared with Ga, leading to a preferential incorporation of Ga in the precipitates. The impact of these precipitates on the wafer bow of the structures is considered.

1. Introduction

Growth on large-area silicon substrates has the potential to significantly reduce the manufacturing cost of GaN-based light emitting diodes (LEDs) and GaN based electronic devices [1]. This is because it enables the use of the high yield, high throughput processing techniques that have been developed for silicon integrated circuits. However, there is a large mismatch in lattice parameters (17%) and thermal expansion coefficients (46%) between Si and GaN, which makes the direct growth of GaN on Si challenging [2]. The mismatch in thermal expansion causes wafer bowing and/or cracking due to a tensile stress built up in the films upon cooling from the growth temperature. A common solution to this is to introduce graded AlGaN intermediate layers, which provide a compressive stress into the epilayer during growth to compensate the tensile stress during cooling [3–5].

The evolution of strain relating to the use of AlGaN buffer layers for stress compensation is complex and still not well understood. To avoid 'melt back' etching by Ga of the Si substrate, the growth generally starts with an AlN nucleation layer. This layer has a large influence on the final stress present in a GaN structure, and its quality is reported to be strongly affected by growth temperature [6], TMA pre-dose time [7], V/III ratio [8] and layer thickness [9,10]. In addition, the compressive stress from utilizing graded AlGaN layers is compromised more or less by the movement of dislocations depending on growth conditions [11]. The stress state in a film may be further modulated by doping elements such as Si and Mg [12,13]. All these suggest that in order to produce crack-free and flat LED structures, the thickness of all the epilayers and their growth conditions need to be precisely engineered as a whole.

In the present work, an attempt has been made to understand the origin of large surface hillocks (also known as pancake defects) observed on the surface of GaN-on-Si structures. As shown in Fig. 1, these defects are $\sim 50\,\mu m$ in diameter and appear with a high density ($\sim 10^4\,cm^{-2}$ estimated from Normarski microscopy images). Atom force microscopy (AFM) measurements show that the height of the hillocks is about 50 nm for a nitride layer thickness of about 2.5 μm. In LEDs, they cause a disruption of the InGaN quantum well growth leading to regions of poor light emission at their edges. Our initial experiment showed that the AlN nucleation layer has a strong effect on the formation of hillocks, since only some AlN templates produce such defects when the growth of all the layers above is kept the same. A systematic study has then been carried out by making a series of GaN-on-Si wafers with a different AlN nucleation layer but the same epilayers on top. These wafers are characterised by x-ray diffraction (XRD) and transmission electron microscopy (TEM). The experimental results bring further insight into the important role played by the AlN nucleation layer, and reveal that a phase separation occurring in the AlGaN buffer layer is the cause of the surface hillocks.

* Corresponding author. Tel.: +44 1223 767930
E-mail addresses: yh241@cam.ac.uk, Yisong.han@gmail.com (Y. Han).

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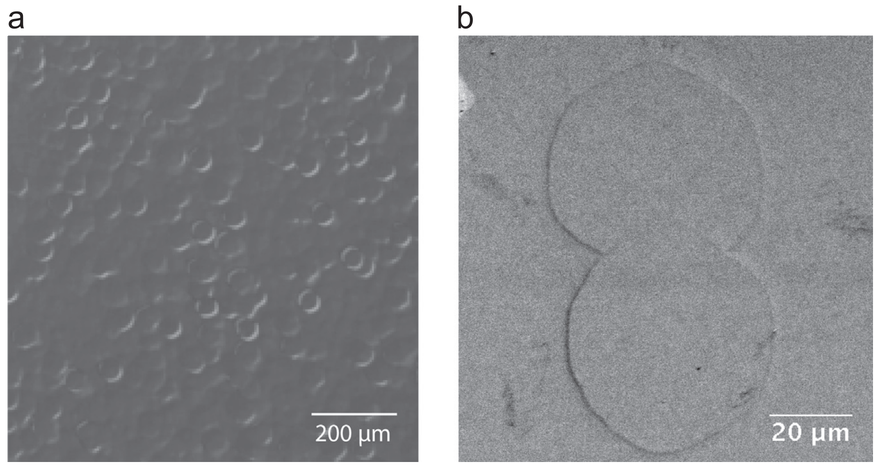

Fig. 1. (a) Normarski microscopy and (b) SEM images of surface hillocks on a GaN wafer grown on Si(111).

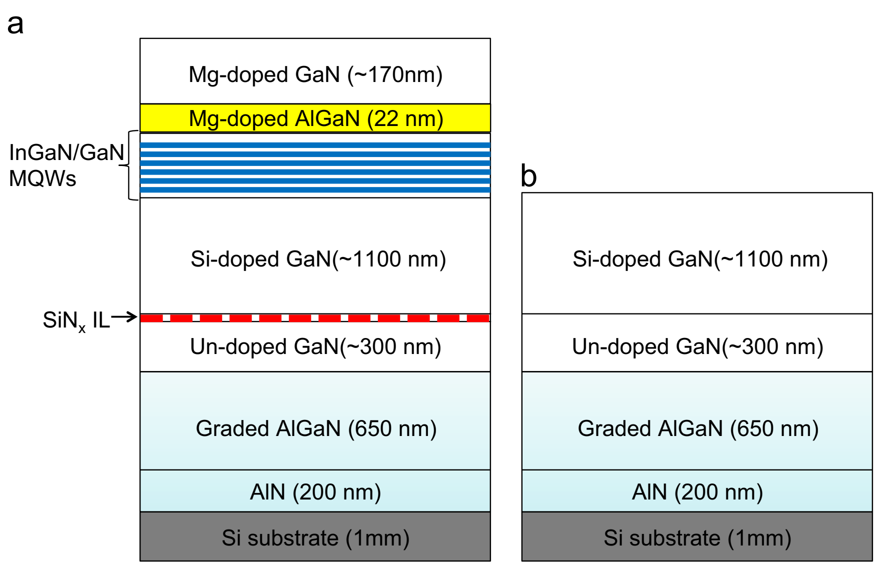

Fig. 2. (a) Layer structure of the GaN-on-Si samples with a SiNx interlayer and a full QW structure. (b) Layer structure of the test wafers.

2. Experimental

All the samples studied were grown on 6 in. Si(111) substrates by metal-organic vapor phase epitaxy (MOVPE) in a 7 × 6" Aixtron close coupled shower-head reactor. TEM investigations were performed on wafers with a full InGaN/GaN LED structure (the structure of these samples is shown in Fig. 2a). In this case, a SiNx interlayer was deposited for dislocation reduction. Since the insertion of a SiNx interlayer and the growth of other layers on top of AlN will also affect the overall stress management, in order to investigate the effect of the quality of AlN, simple GaN test wafers were also prepared (see Fig. 2b). The epitaxial growth of the test wafers was carried out in two steps: firstly, AlN layers were grown under different growth conditions and characterised using XRD and AFM; secondly, these AlN templates were reloaded into the reactor for the growth of the subsequent compositionally continuously graded AlGaN and GaN layers. For each growth run, up to 5 different AlN templates along with a "standard" template were loaded in to the growth reactor. The similar properties of the "standard" template layer in each growth run give confidence that the growth conditions of the AlGaN/GaN layer were accurately reproduced and that the growth interruption is not significantly changing the stress in the layers. To avoid any contamination issues, carrier baking and showerhead cleaning were conducted after each run following a standard procedure.

X-ray diffraction measurements were performed using a Panalytical high-resolution diffractometer on the AlN nucleation layers before growing other epilayers on top. The peak width (FWHM, full width at half maximum) of AlN was acquired by an ω-scan on the (002) and (101) reflections and gives information about the tilt and twist respectively of the crystal planes in the layers. The wafer bow was measured *ex-situ* using an E+H Metrology MX203 Wafer Geometry Gauge. Cross-sectional thin foils were prepared by focused ion beam (FIB) right at the center of the hillocks for TEM observations. TEM diffraction contrast images were recorded in a CM30 microscope, operated at 300 kV. Annular dark-field imaging (ADF) was carried out in an FEI Tecnai Osiris microscope, operated at 200 kV. Energy dispersive X-ray spectroscopy (EDX) spectra were acquired under STEM mode using Bruker silicon drift detectors (SDD) attached to the Osiris microscope.

3. Results and discussion

Fig. 3 shows the appearance of surface hillocks and the bowing of the GaN test wafers (see Fig. 2b) with reference to the XRD