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Thickness influence of thermal oxide layers on the formation of self-catalyzed InAs nanowires on Si(111) by MOCVD

Xiaoye Wang, Xiaoguang Yang, Wenna Du, Haiming Ji, Shuai Luo, Tao Yang *

Key Laboratory of Semiconductor Materials Science, Institute of Semiconductors, Chinese Academy of Sciences, Beijing 100083, People's Republic of China

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ABSTRACT

The thickness influence of thermal oxide layers on Si(111) substrates on the formation of self-catalyzed InAs nanowires (NWs) grown by metal-organic chemical vapor deposition (MOCVD) has been investigated. It is found that the thickness of the thermal oxide layer has a strong effect on the morphological characteristics of InAs NWs formed on the Si substrates. In particular, within a suitable thickness range, it is possible to achieve vertical InAs NWs with a uniform distribution of their positions, lengths and diameters. In addition, growth on the thermal oxide layer both improves the morphology of the NWs, and suppresses the frequently observed parasitic islands compared to growth on bare Si. A growth model, which is based on the diffusion length of adatoms, the growth temperature, the thickness of thermal oxide layer, the size and the density of thermal oxide holes, has been developed to explain the formation of the self-catalyzed InAs NWs on the Si substrate with a thermal oxide layer.

1. Introduction

III–V semiconductor nanowires (NWs) have attracted considerable attention because of their unique electronic and optical properties as well as their potential applications in high-performance electronic and optoelectronic nanodevices. The narrow diameter of NWs permits the NWs' lattice to radially shrink or extend at the interface between the NWs and the substrate, and so that the strain between the lattice-mismatched materials can be relieved without causing strain-relieving misfit dislocations [1,2]. So far, various prototype devices of III–V NWs, especially using InAs, have been demonstrated, such as gas sensors [3], single-electron transistors [4], resonant-tunneling diodes [5], tunneling field-effect transistors [6], field-emission sources [7], charge detectors [8] and other high-speed electronic devices [9]. The possibility of fabricating vertical InAs NWs on Si substrates allows the integration of high-speed InAs electronic devices with modern CMOS technology. This combines the advantages of InAs high electron mobility and of small electron effective mass with the manufacturability of a standard CMOS technology.

The main methods used to grow NWs include Au-catalyzed growth [10], self-catalyzed growth [11] and catalyst-free selective-area growth [12]. In most cases, metal seed particles, preferably Au nanoparticles, are widely used as catalysts for the growth of NWs. Considering the practical applications, the Au-catalyzed growth of NWs has some disadvantages. For example, Au contamination will introduce impurities in the NWs and unwanted deep-level recombination centers in the Si substrate, resulting in adverse effects on the electronic and optoelectronic nanodevices based on the NWs.

In contrast, self-catalyzed growth has many advantages over Au-catalyzed growth. Since there is no need to deposit Au aerosol nanoparticles on the substrate, simplified and low-cost manufacturing process of the NWs can be achieved and Au contamination can be avoided. Also the growth temperature (around 550 °C) for the self-catalyzed InAs NWs is higher than that for Au-catalyzed growth (350–500 °C) [13,14], it can reduce the carbon contamination that results from the CH_4 produced in the MOCVD process [15,16].

Many mechanisms have been used to interpret the growth process of the NWs, such as vapor–liquid–solid (VLS) [10], vapor–solid–solid (VSS) [17,18], solution–liquid–solid (SLS) [19] and solid–liquid–solid [20] mechanisms, but they are still under discussion. Most of relevant studies center on the influence of the growth conditions on the formation of the NWs. There is little work on the effect of substrate surfaces on the growth of NWs.

In this work, the thickness influence of a thermal oxide layer on the growth of the self-catalyzed InAs NWs on the Si(111) substrates is reported, including the suppression of the growth of large parasitic islands. A model, which combines the diffusion length of adatoms, the growth temperature, the thickness of

* Correspondence to: Institute of Semiconductors, CAS P.O. Box 912, Beijing 100083, People's Republic of China. Tel./fax: 86 10 82304529.
E-mail address: tyang@semi.ac.cn (T. Yang).

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thermal oxide layer, the size and the density of thermal oxide holes, is presented to explain the growth process of the InAs NWs, the mechanism of controlling NWs' density and diameter, and the mechanism of suppressing the growth of large parasitic islands.

2. Experimental section

Self-catalyzed InAs NWs have been grown on p-type Si(111) substrates by a close-coupled showerhead, low-pressure MOCVD system (AIXTRON Ltd., Germany), using ultra-high purity H_2 as a carrier gas, and trimethylindium (TMIn) and AsH_3 as gas precursors. The chamber pressure during the growth was 133 mbar, and the total flow of H_2 was 12 slm. The substrates were first heated in situ to 635 °C for annealing and then cooled down to 400 °C. The temperature was raised to the growth temperature 550 °C in an AsH_3-rich (2.0×10^{-4} mol/min) environment, and after a short stabilization time, NW growth was initiated by introducing the TMIn (2.0×10^{-6} mol/min) for 7 min and stopped by switching off the TMIn source. Finally, the substrates were cooled down in an AsH_3 ambient. The morphology of InAs NWs was characterized using scanning electron microscopy (SEM).

Table 1
The samples with thermal oxide layers of different thicknesses.

Samples	A	B	C	D	E	F
Thickness (Å)	66	46	27	9	2	0

3. Results and discussion

3.1. NWs' morphology characteristic

First, the influence of a thermal oxide layer on the formation of the self-catalyzed InAs NWs on the Si(111) substrate was investigated. To do this, the Si substrates with 20 nm-thick thermal oxide layers were etched in a 1.9% aqueous hydrofluoric (HF) acid solution for different time to achieve thermal oxide layers of different thickness. The thickness of the thermal oxide layers was measured using ellipsometry. The details of the samples used in this study are listed in Table 1. After etching, the substrates were rinsed in DI water for 20 s and dried with N_2 before growth.

Fig. 1 shows SEM images of the InAs NWs grown on the Si substrates with thermal oxide layers of different thicknesses. Note that the sample of which thermal oxide layer's thickness is 0 (Table 1) corresponds to the bare silicon substrate (sample F). It can be easily seen that vertical InAs NWs with a more uniform distribution (Fig. 1a–e) can be obtained, compared with those grown on the bare Si substrate (Fig. 1f). Furthermore, the parasitic islands (Fig. 1a–e) which frequently appear, as shown in Fig. 1f,

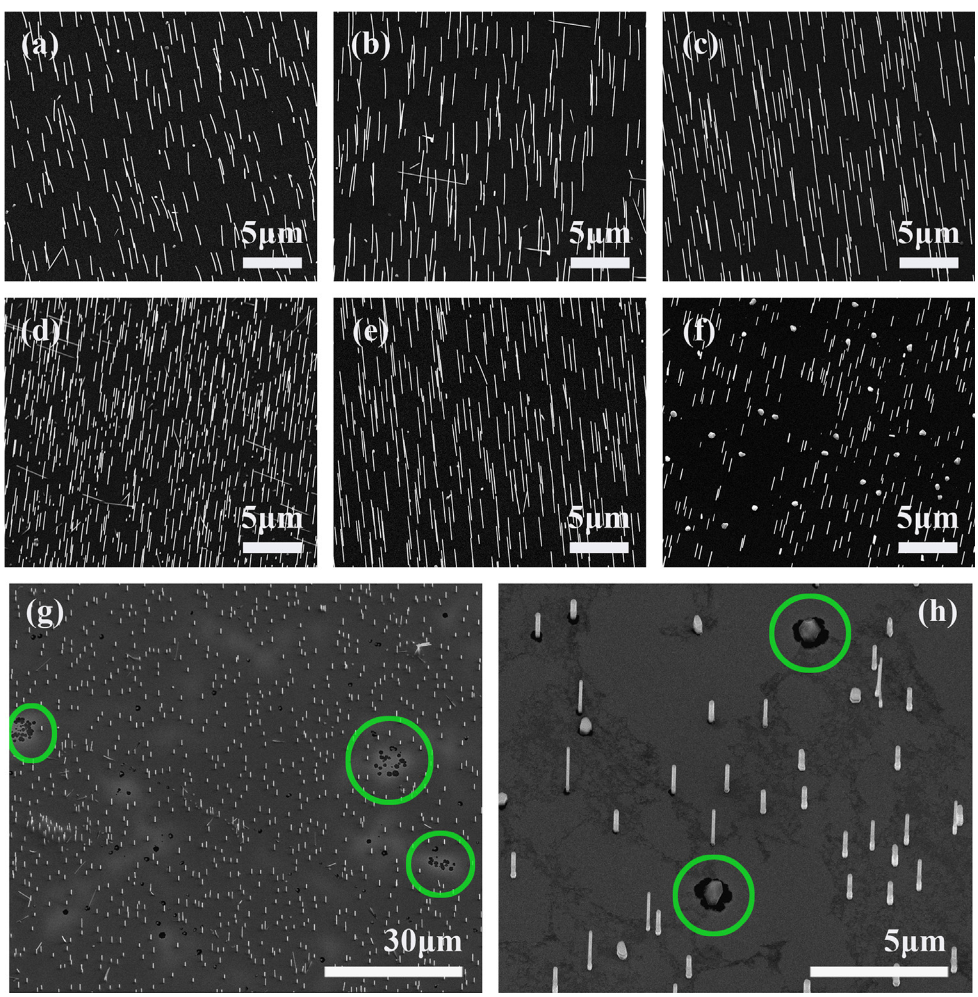

Fig. 1. (a–f) SEM images of InAs NWs grown on Si(111) substrates with thermal oxide layers of different thicknesses: (a) 66 Å, (b) 46 Å, (c) 27 Å,(d) 9 Å, (e) 2 Å and (f) 0 Å. All images are viewed at a tilt of 30° from the surface normal. (g, h) SEM images of the sample coated with PMMA and then processed by an etching step. It appears many large areas of collapsed holes at the site of the parasitic islands, which are marked by green circles. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)