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Low-temperature growth of epitaxial (1 0 0) silicon based on silane and disilane in a 300 mm UHV/CVD cold-wall reactor

T.N. Adam [a,*], S. Bedell [a], A. Reznicek [a], D.K. Sadana [a], A. Venkateshan [b], T. Tsunoda [b], T. Seino [c], J. Nakatsuru [c], S.R. Shinde [b]

[a] IBM Research, 1101 Kitchawan Road, Yorktown Heights, NY 10598, USA
[b] Canon ANELVA Corporation, 3300 North First Street, San Jose, CA 95134, USA
[c] Canon ANELVA Corporation, 5-1 Kurigi 2 choume, Asao-ku, Kawasaki-shi, Kanagawa 215-8550, Japan

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ABSTRACT

Epitaxial (1 0 0) silicon layers were grown at temperatures ranging from 500 to 800 °C in a commercial cold-wall type UHV/CVD reactor at pressures less than 7×10^{-5} Torr. The substrates were 300 mm SIMOX SOI wafers and spectroscopic ellipsometry was used to assess growth rates and deposition uniformities. High-resolution atomic force microscopy (AFM) was employed to verify the atomic terrace configuration that resulted from epitaxial step-flow growth. Deposition from disilane exhibited a nearly perfect reaction limit for low temperatures and high precursor flow rates (partial pressures) with measured activation energies of $\approx$2.0 eV, while a linear dependence of growth rate on precursor gas flow was found for the massflow-controlled regime. A similar behavior was observed in the case of silane with substantially reduced deposition rates in the massflow-limited regime and nearly a factor of 2 reduced growth rates deep in the reaction limited regime. High growth rates of up to 50 μm/h and non-uniformities as low as $1\sigma=1.45\%$ were obtained in the massflow-limited deposition regime. Silicon layers as thin as 0.6 nm (4.5 atomic layers) were deposited continuously as determined using a unique wet chemical etching technique as well as cross-sectional high-resolution transmission electron microscopy (HRTEM). In contrast, epitaxial silicon deposited in RPCVD at 10 Torr using disilane within the same temperature range showed imperfect reaction limitation. While activation energies similar to that of UHV/CVD were found, no partial pressure limitation could be observed. Furthermore, layers deposited using disilane in RPCVD exhibited a large number of defects that appeared to form randomly during growth. We attribute this effect to gas phase reactions that create precursor fragments and radicals—an effect that is negligible in UHV/CVD.

1. Introduction

As device dimensions of modern state-of-the-art CMOS and HBT technologies continue to shrink in the race to faster and less power consuming transistors and circuits, unrivalled demands on various fabrication sectors and processes prolong the development learning cycle time, diminish the success rate, and consequently result in a substantially increased cost. Besides lithography, the areas that are affected the most are thin-film deposition, ion implantation, and processing, where high-temperature steps are required. One such high-temperature process is the deposition of epitaxial films, especially selective to SiO_2 and Si_3N_4, where growth temperatures were traditionally as high as 950 °C. Even though continued advances in tooling and precursor development resulted in the ability to reduce growth temperatures below 650 °C for selective processes, deposition times remain excessive and high thermal budgets for in situ pre-growth substrate "baking" are still required. In addition, purity of the reactor environment as well as carrier and precursor gases in the atmospheric (760 Torr), reduced (1–600 Torr), and low pressure (0.1–1 Torr) regime would require trace levels of water and oxygen vapor in low parts per billion (ppb) and below to continue this trend of reducing growth temperatures [1,2]. It is apparent that the complexity and cost of an epitaxial group-IV CVD system are going to continue to increase in the quest to minimize effects of high-temperature processing on device performance, such as dopant diffusion, strain relaxation, and alloy intermixing that result in degraded electrical performance. Currently, the majority of CVD systems employed in production facilities operate at atmospheric, reduced, or low pressures due to a simple and low-cost reactor and pumping system design. In this paper, we present UHV/CVD as an alternative to the conventional epitaxial group-IV CVD. In this work, we explore undoped epitaxial

* Corresponding author.
E-mail addresses: tadam@us.ibm.com (T.N. Adam), aarthi.venkateshan@canon-anelva.com (A. Venkateshan), shinde.sanjay@canon-anelva.com (S.R. Shinde).

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silicon growth in the full temperature range available to a commercial UHV/CVD tool [3] and show the advantages and drawbacks as compared to RPCVD.

2. Experimental

Epitaxial silicon layers were deposited in a commercially available cold-wall stainless steel UHV/CVD reactor depicted in Fig. 1 at substrate temperatures ranging from 500 °C to a maximum allowed temperature of 800 °C. Lower temperatures were possible; however, growth rates quickly diminished below 500 °C for Si_2H_6 (525 °C for SiH_4). The reactor background pressure was 5×10^{-9} Torr or better and care was taken to maintain a process pressure less than 7×10^{-5} Torr during deposition in order to maximize the precursor mean free path and thus minimize gas phase reactions. Undiluted high-purity (1 ppmv $H_2O/O_2/CO/CO_2$) Si_2H_6 or SiH_4 was injected without purifiers through calibrated massflow controllers, and high-speed turbo-molecular pumps ensured pressures less than 7×10^{-5} Torr during gas flow. To minimize the amount of contamination introduced during wafer loading, the deposition chambers were attached to a UHV transfer-chamber platform equipped with UHV loadlocks and UHV compatible wafer handling robots. The main frame layout as depicted on the right hand side of Fig. 1 is configurable with one or more transfer chambers that allow for in situ clustering of different types of UHV stations, such as oxidation, annealing, PVD, and CVD reactors. Typically, wafers were loaded from atmosphere to 1×10^{-7} Torr within less than 10 min. The deposition chambers were water-cooled stainless steel reactors that were equipped with graphite susceptors having multi-zone heaters, an optimized precursor injection system designed for homogeneous gas delivery, thermo-couple (TC; in the vicinity of susceptor) and pyrometer (directed at the wafer surface) temperature sensors, and a recipe-driven control that was fully integrated with the fabrication line automation system. Two separate turbo pumps were used to evacuate the reactor volume and heater–susceptor assembly in order to avoid reactants from entering the heater space. Each chamber was equipped with open-loop pressure regulation consisting of a variable conductance orifice. However, all experiments presented here were conducted using the highest conductance (orifice fully open) to ensure the lowest deposition pressures. Hot ionization gauges were used to measure heater chamber pressures at all times, including during deposition. Wafers were loaded into the reactors notch-aligned and remained stationary during deposition (i.e. not rotated). True wafer temperatures were calibrated weekly by measuring the TC-to-pyrometer temperature offset for a TC temperature range of 650–950 °C. In addition, the silicon growth rate was validated by growing a SiGe–Si stack, which eliminated nucleation and interface contamination related changes.

Prior to deposition, the system was inspected for vacuum leaks using a helium mass-spectrometer-type analyzer as well as a residual gas analyzer permanently attached to the deposition chamber. The wafers were blanket (un-patterned) unprocessed 300 mm SOI substrates (SIMOX-type with 50 nm upper Si thickness) that were re-used until the top silicon thickness exceeded 250 nm, where spectroscopic ellipsometry measurements became unstable. The as-received wafers were chemically cleaned in an HF dip targeted for 55 Å thermal SiO_2 removal followed by a water rinse and isopropyl dry. Typical queue times (between the end of pre-clean and load-start at the UHV/CVD tool) were between 2 and 60 min. A "high" temperature in situ pre-bake was performed under ultra-high vacuum at temperatures between 700 and 750 °C immediately prior to deposition for 2–3 min to desorb the remaining sub-stoichiometric surface oxide that reformed during exposure to air. This combination of pre-clean and in situ pre-bake resulted in very low values of interface contamination dose determined by integrating the SIMS intensity under the interface peak. Oxygen doses were typically below the detection limit ($<1\times10^{12}\,cm^{-2}$) while small amounts of carbon in the order of $<2\times10^{12}\,cm^{-2}$ were sometimes detected. All growth rates were extracted by measuring the top silicon thickness before and after deposition on a 52-point Cartesian map in a spectroscopic ellipsometer [4] resulting in a 38 mm data spacing. The "goodness-of-fit" (GOF) extracted from a least-square fitting routine was monitored for every measurement point to ensure the validity of the measurement. Generally, the SIMOX wafers were repeatedly used for deposition until GOF had reduced 25% (from near 1 to 0.75).

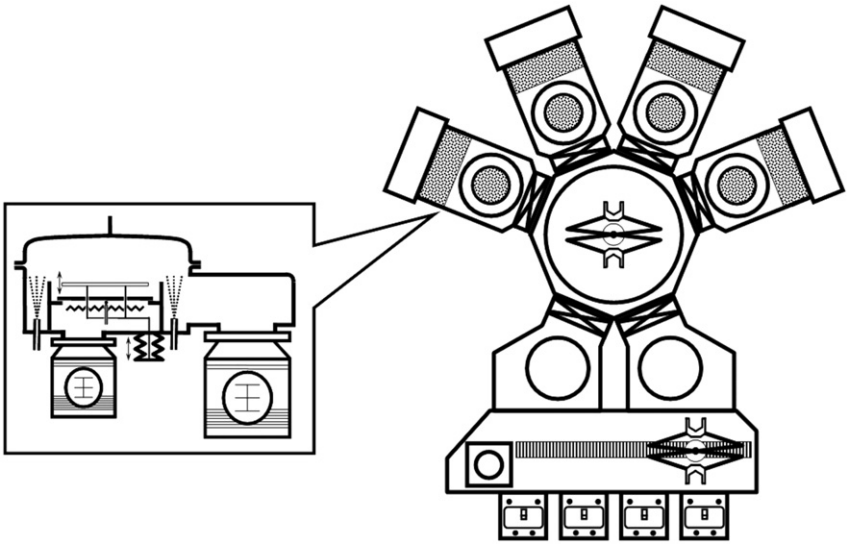

Fig. 1. Schematic depiction of the UHV/CVD chamber and reactor employed in this study. Two concurrently evacuating turbo pumps ensure the lowest pressures in both the reaction chamber and heater space (left image). Multiple UHV processing chambers were attached to a UHV transfer main frame designed for minimal exposure to ambient (right image). The layout is configurable with one or more transfer chambers, allowing in situ clustering of various high-vacuum processing chambers, such as CVD, PVD, oxidation, or annealing stations.