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Growth kinetics of SiGe/Si superlattices on bulk and silicon-on-insulator substrates for multi-channel devices

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ABSTRACT

We have studied in reduced pressure chemical vapor deposition the growth kinetics of Si and $Si_{0.8}Ge_{0.2}$ on bulk Si(0 0 1) and on silicon-on-insulator (145 nm buried oxide/20 nm Si over-layer) substrates. For this, we have grown at 650 °C, 20 Torr 19 periods ($Si_{0.8}Ge_{0.2}$ 19 nm/Si 32 nm) superlattices on both types of substrates that we have studied in secondary ion mass spectrometry, X-ray diffraction and cross-sectional transmission electron microscopy. The Si and SiGe growth rates together with the Ge content are steady on bulk Si(0 0 1), with mean values around 9.5 nm min^{-1} and 20.2%, respectively. In contrast, growth rates decrease from ~9.5 nm min^{-1} down to values around 7.0 nm min^{-1} (SiGe) and 6.3 nm min^{-1} (Si), when the deposited thickness on SOI increases from 0 up to slightly more than 100 nm. They then go back up to values around 8.8–9.0 nm min^{-1} as the thickness increases from 100 up to 400 nm. They then slowly decrease to values around 8.4–8.6 nm min^{-1} as the thickness increases from 400 up to 800 nm. The Ge concentration follows on SOI exactly the opposite trend: an increase from 19.9% (0 nm) up to 20.6% (~100 nm) followed by a decrease to values around 20.1% (400 nm) then a slow re-increase up to 20.4% (800 nm). These fluctuations are most likely due to the following SOI surface temperature variations: from 650 °C down to 638 °C (100 nm), back up to 648 °C (400 nm) followed by a slow decrease to 646 °C (800 nm). These data curves will be most useful to grow on conventional SOI substrates large number of periods, regular $Si/Si_{0.8}Ge_{0.2}$ superlattices that will serve as the core of multi-channel or three-dimensional nano-wires field effect transistors.

1. Introduction

In order to meet the high-performance requirements of the ITRS roadmap after 2010, a large number of non-classical architectures for metal oxide semiconductor field effect transistors (MOSFETs) have quite recently been proposed, with promising electrical performances. Of note are the double-gate [1], the localized silicon-on-insulator (L-SOI) [2], the silicon-on-nothing (SON) [3], the multi-channel (MC) [4,5] and the three-dimensional nano-wires (3D-NW) [6–8] devices. They all rely on (i) the (selective) epitaxy of SiGe/Si multilayers [9–11], (ii) the anisotropic etching of the active area [12] and (iii) the high degree of selectivity (versus Si) that can be achieved when laterally etching the SiGe layers (with Ge contents above 15%) [13–17]. In the L-SOI and SON approaches, the voids left by the removal of the SiGe buried layer are filled by a Si_3N_4/SiO_2 sandwich, leading to the formation of FETs (with localized buried dielectric layers beneath the Si surface channel/gate stacks) that electrically operate in a fully depleted-like regime. In the MC (the 3D-NW) case, the suspended Si slabs (the matrices of suspended Si nano-wires) left after the selective dry etching of the SiGe layers are encapsulated in a conformal fashion by HfO_2/TiN/poly-Si gates, leading to the formation of multi-channel devices. MC and 3D-NW devices offer great potential for ultimate MOSFET down-scaling. Indeed, they provide a current density per area which is directly proportional to the number of stacked channels, a double-gate or gate-all-around-like electrostatic control of each channel by the gate, self alignment of the channels, gate and junctions, the design flexibility of planar devices, etc. The best I_{ON}/I_{OFF} trade-offs so far have recently been obtained in MC-FETs [5]: I_{ON}=2.27 mA/μm ⇔ I_{OFF}=16.4 pA/μm (nMOS) and I_{ON}=1.32 mA/μm ⇔ I_{OFF}=16.75 pA/μm (pMOS). Extremely high I_{ON} currents for reasonable I_{OFF} currents have very recently been achieved in 3D-NW FETs: I_{ON}=6.5 mA/μm ⇔ I_{OFF}=27 nA/μm (nMOS) and I_{ON}=3.3 mA/μm ⇔ I_{OFF}=0.5 nA/μm (pMOS) [8].

The MC and 3D-NW integration schemes call upon the epitaxial growth of SiGe/Si superlattices either on bulk or on silicon-on-insulator (SOI) substrates. We have thus investigated the specifics of the reduced pressure-chemical vapor deposition (RP-CVD) of Si and SiGe on both types of substrates. Some limited literature data have indeed shown that the Si growth rate can either increase [18] or decrease [19,20] when switching from bulk

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to SOI substrates. Both the buried oxide thickness and the over-layer thickness seem to have an impact on it [19,20], hinting at changes in surface temperature depending on the stack. Such variations would (if not corrected) dramatically degrade the period reproducibility of SiGe/Si superlattices grown on SOI substrates.

2. Experimental details

We have used an Epi Centura RP-CVD industrial cluster tool manufactured by applied materials to grow all the structures studied in this paper. The platform is constituted of six interconnected chambers: two load-lock chambers that can hold up to twenty five 200 mm wafers, a transfer chamber that acts also as a buffer chamber and contains the robot for wafer transferring, a cool-down–wafer-centering chamber and two RP-CVD growth chambers. The samples were either grown on lightly p-type-doped Si(0 0 1) bulk substrates or on {20 nm Si over-layer/145 nm BOX} SOI substrates. The growth pressure was *always* 20 Torr. The flow of H_2 carrier gas was set at a *fixed value* of a few tens of standard liters per minute, which was *not* altered throughout all the experiments. Pure dichlorosilane (SiH_2Cl_2) or silane (SiH_4) were used as the source of Si and germane (GeH_4) diluted at 2% in H_2 as the source of Ge. Temperature monitoring and control was ensured through the lower pyrometer, i.e., the one which is looking at the backside of the susceptor plate on which the wafer lies (see Fig. 1). The reading is therefore independent of the nature of the substrate (i.e., bulk or SOI). The high-resolution X-ray diffraction (XRD) experiments were performed on a panalytical X'pert diffractometer. The secondary ion mass spectrometry (SIMS) measurements were carried out on a Cameca IMS 5f apparatus. Cs^+ primary ions were used for silicon and germanium depth profiling, with a 2 keV impact energy. The atomic masses monitored were those of $Cs_2^{28}Si^+$ ($133\times2+28=294$ amu) and $Cs_2^{70}Ge^+$ ($133\times2+70=336$ amu) [21,22]. Finally, the cross-sectional transmission electron microscopy (TEM) images were acquired at 200 kV on a Akashi EM 002B microscope (with an ultra-high-resolution pole piece).

3. The samples grown and measurement protocol used

In order to quantify the growth kinetics changes occurring when switching from bulk to SOI, we have (after an "HF-last" wet cleaning followed by an in-situ 850 °C, 2 min H_2 bake) grown on both types of substrates 19 periods {$Si_{0.8}Ge_{0.2}$/Si} superlattices using the *very same recipe*. The nominal $Si_{0.8}Ge_{0.2}$ and Si layer thickness were equal to 19 and 32 nm, respectively. The $Si_{0.8}Ge_{0.2}$ layers were grown at 650 °C using a SiH_2Cl_2 ($F(SiH_2Cl_2)/F(H_2)=0.0025$) and GeH_4 ($F(GeH_4)/F(H_2)=8.33\times10^{-5}$) chemistry [20]. Such a low-growth temperature indeed enables to grow quite thick SiGe layers without any elastic relaxation of the strain through the formation of surface undulations [20,23,24]. The Si layers were also grown at 650 °C using SiH_4 ($F(SiH_4)/F(H_2)=0.01$).

We have used high-resolution XRD to study the 19 periods SL grown on bulk Si(0 0 1). We have the presence on the $\omega-2\theta$ profile around the (0 0 4) diffraction order of numerous well defined and intense SL satellite peaks on each side of the Si substrate peak (see Fig. 2). Their angular spacing is inversely proportional to the *SL period* (i.e., the thickness of the SiGe/Si bi-layer), while the angular position of the 0th order peak (compared to the Si substrate peak) is dictated by the *mean Ge concentration in a period*. Numerous small thickness fringes, whose angular spacing is inversely proportional to the *overall SL thickness*, are also present between satellite peaks. They testify to the excellent crystalline quality of the stack and to the abruptness of the SiGe/Si interfaces. We are thus most likely below the critical thickness of plastic relaxation [25] of the individual compressively strained $Si_{0.8}Ge_{0.2}$ layers and of the overall {$Si_{0.8}Ge_{0.2}$/Si} SL. This conclusion is supported by the smooth, featureless surface morphology observed in tapping mode atomic force microscopy (see [11] for more details). The

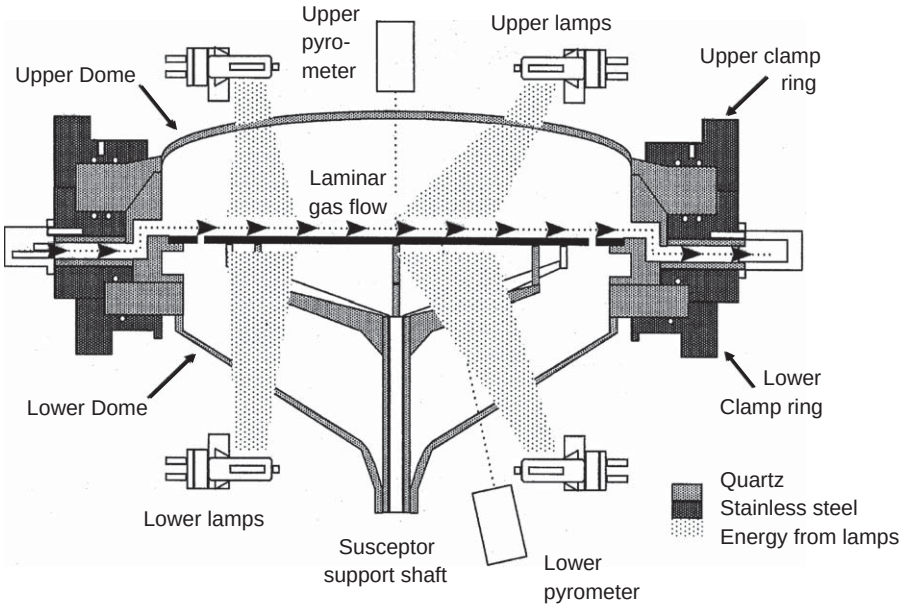

Fig. 1. The applied materials 200 mm Epi Centura chamber is physically limited by upper and lower transparent quartz domes (light grey) which are clamped onto a metallic base plate, thanks to metallic rings (dark grey) which compress seals (small circles on each side of the chamber). Chamber tightness is thus insured, with a few mTorr base pressure and several tens of μTorr/min leak rates. The wafer lies horizontally on top of a graphite plate (coated with SiC) that rotates (30 laps/min) during growth to improve thickness uniformity (thick horizontal black line in the schematics). Gaseous precursors are delivered (through quartz inserts) in a laminar fashion just above the wafer surface (arrows). Their thermal decomposition is achieved using two banks of twenty 2 kW lamps (8 pointing towards the wafer center and 12 towards the edges, as symbolized by dotted beams). Temperature is controlled by two infra-red pyrometers, one looking directly at the wafer surface and the other at the back of the susceptor plate on which the wafer lies. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)