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Role of thermal expansion matching in CdTe heteroepitaxy on highly lattice-mismatched substrates

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ABSTRACT

We report on the significance of thermal expansion mismatch in the heteroepitaxial growth of CdTe on highly lattice-mismatched substrates. Such substrates including Si, Ge, or GaAs are desirable for CdTe buffer layer growth and subsequent deposition of HgCdTe infrared absorber layers. Besides lattice misfit, the thermal mismatch associated with these systems can produce additional strain and defects at low or elevated temperatures. However, little work has been done towards documenting and understanding these effects. Experimental evidence of thermal-expansion-dependent residual stress is presented for CdTe/Si(211), CdTe/Ge(211), and CdTe/GaAs(211) films based on X-ray diffraction studies. The experimental results are also compared with residual stress calculations based on known material properties. These results may play a vital role in the design and development of HgCdTe detectors for large-format, infrared focal plane arrays (FPA).

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1. Introduction

High crystalline quality semiconductor thin films are deposited on similarly lattice and thermally matched substrates. One such application is that of HgCdTe-based infrared (IR) detectors for which lattice-matched CdZnTe (CZT) substrates have traditionally been used. Although CZT is an ideal match to the HgCdTe overlayers, it is not ideal from the standpoint of its commercial availability in relatively small sizes. In addition, efforts to grow defect-free bulk CZT have been met with limited success. With growing interest in a larger-area substrate for HgCdTe epitaxy, CdTe/Si composite substrates have received significant attention despite an unprecedented 19% mismatch in the film-substrate lattice parameter [1–5]. Due to the much smaller lattice mismatch for CdTe and $Hg_{1-x}Cd_xTe$ (where composition x is tuned for detection of particular IR wavelengths), it is the CdTe/Si interface that is primarily responsible for lattice defects. The CdTe buffer layer is typically deposited via molecular beam epitaxy (MBE) to thickness of 8–12 μm on As-passivated Si(211) substrates. This thickness is required to limit (via interaction and annihilation) the high densities of lattice-mismatch induced dislocations from reaching the surface and threading into subsequently grown HgCdTe device layers. As-passivation of the Si(211) surface has been successfully employed to promote the growth of B-phase (Te-terminated) CdTe films, which are preferred for HgCdTe devices. In addition, the (211) substrate orientation has been proven for HgCdTe epitaxy as a means to suppress twinning defects and surface hillocks [3,5].

Despite the demonstration of good-performing devices for short and mid-wavelength IR detection using CdTe/Si substrates, similar successes for long-wavelength ($\geqslant$9.5 μm) detection have been difficult to realize. Most reports appropriately fault the large lattice mismatch typically associated with structural defects that can reduce device performance [6,7]. Nonetheless, debate continues as to the relevance of other materials issues including thermal expansion mismatch, which may also contribute to large

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dislocation densities and other important defects. CdTe buffered Ge [8,9] and GaAs [10,11] have also been examined as low-cost, large-area alternative substrates, and may each have distinct advantages over Si. Table 1 lists material properties of interest for the three substrates. Ge has been an attractive alternative to Si due to better lattice and thermal expansion (α) matching to CdTe and also because it is compatible with Si processing equipment. An almost equally better lattice and thermal expansion match to CdTe is provided by GaAs substrates. GaAs may also provide an extra benefit due to its zinc-blend structure and thus naturally polar (211) surface, on which achieving uniform B-phase CdTe(211) should be more straightforward.

The material properties listed in Table 1 suggest an opportunity to examine the relevance of thermal expansion in highly lattice-mismatched materials. Here, we investigate the effects of thermal expansion in MBE-grown CdTe/Si, CdTe/Ge, and CdTe/GaAs heteroepitaxial structures. Initial and residual thin film stresses are predicted from theory based on known material properties. The overall residual film stress is measured by X-ray diffraction (XRD) and surface profilometry methods, and then compared to theoretically predicted values for the individual contributions of stress from lattice and thermal mismatch. Finally, temperature-dependent lattice parameter measurements via XRD are performed. Analysis of these results leads to important conclusions concerning the effects of thermal expansion in epitaxial systems with large lattice mismatch.

2. Experiment

The technology for state-of-the-art CdTe/Si(211) composite substrates by molecular beam epitaxy has been developed at the Night Vision and Electronic Sensors Directorate [1,2]. Si(211) wafer surfaces are hydrogen passivated ex-situ using an HF-based solution. Upon loading the Si substrate into the MBE chamber (VG80H, Oxford Instruments), hydrogen is desorbed while ramping to approximately 800 °C and exposing the surface to an As_4 flux. This produces an atomic layer of As, which is used to promote the subsequent growth of B-oriented ZnTe/CdTe at 390 °C [12]. The thin (~150 Å thick) ZnTe film has been used as a seeding layer and will not be considered during stress calculations. The CdTe film is typically between 8 to 12 μm thick and is thus expected to dominate the film stress characteristics in the composite substrate. When periodic anneals (~560 °C) are incorporated into the growth recipe, state-of-the-art CdTe/Si(211) composite substrates are achieved. The best CdTe films typically have X-ray rocking curve full-width-at-half-maximum (FWHM) values less than 100 arcsec, and dislocation densities (measured via defect decoration etching) in the mid $10^6\,cm^{-2}$ range. The overall structure of the growth surface is monitored in-situ by reflection high-energy electron diffraction (RHEED). In addition, a quadrupole mass analyzer has been used to identify desorbed species at various stages. The thickness for all films in this study has been determined by Fourier transform infrared spectroscopy (FTIR).

Ge(211) wafers were prepared using an HF-based cleaning technique identical to that used for Si. Chemical surface analysis techniques including X-ray photoelectron spectroscopy (XPS) were employed to verify both H passivation and subsequent As passivation of the Ge surface. RHEED monitoring showed an evolving surface structure during CdTe growth (at ~350 °C), similar to that of growth on Si.

Epi-ready GaAs(211)B wafers were directly loaded into the MBE chamber where the native oxide was thermally desorbed under an As_4 flux. XPS analysis (performed in an adjacent chamber) has been used to verify removal of O and contaminants such as C. In addition, RHEED analysis indicated the (2×1) GaAs surface structure. CdTe was then deposited at 410 °C, after ramping down the substrate from the oxide desorption temperature. It should be noted that substrate temperatures reported in this work are based on thermocouple measurements. In addition, un-annealed CdTe/Ge and CdTe/GaAs samples have been used in order to simplify residual stress analysis.

Etch pit density measurements via the Everson technique [13] were used to examine CdTe films after deposition and after thermal cycling experiments. Residual stress measurements were made using X-ray (Bede D1 X-ray diffractometer) and surface profilometry (Dektak 8) techniques. Out-of-plane thermal expansion coefficient data were obtained using a high-resolution X-ray diffractometer with Cu-Kα radiation from an 18 kW rotating anode generator. Samples were mounted on a metal plate where the stage was appropriately shielded with thermally insulating alumina strips to reduce the temperature gradient between the surface of the sample and the sample holder. The estimated temperature difference between the surface of the sample and the sample holder was within ±2 °C. The temperature was measured by a 100 Ω, platinum room temperature detector (RTD), which was attached to the surface of the sample holder. The temperature was controlled to within ±1 °C by means of a temperature controller with RTD input and a DC output to drive a resistive foil heater placed on the back of the sample holder.

3. Results and discussion

Growth characteristics including film thickness, X-ray FWHM, and etch pit density (EPD) are listed for a number of samples in Table 2. As mentioned earlier, periodic annealing at appropriate temperatures produces the best quality CdTe/Si films (with X-ray FWHM values below 100 arcsec and EPD in the mid $10^6\,cm^{-2}$ range). Though we have not yet achieved such values for growth on Ge and GaAs substrates, similar quality films have been reported in the literature [8–11]. Full optimization of our CdTe/Ge and CdTe/GaAs structures may require further fine-tuning of growth and annealing temperatures. Nonetheless, we have obtained similar quality un-annealed films as evidenced by samples C6048 and C6046 (see Table 2). These films were similar in terms of both X-ray FWHM and surface morphology. Fig. 1 shows Nomarski micrographs of defect decoration etched regions of each sample. From such images, nearly identical etch pit

Table 1
Lattice parameter and thermal expansion coefficient α, for selected substrates of interest for HgCdTe/CdTe epitaxy

Substrate	Crystal structure	Lattice parameter (Å)	Lattice misf (w/CdTe) (%)	α (10^{-6}/C)	α -mismatch (w/CdTe) (%)
Si	Diamond	5.43	−19.3	2.6	−92.3
Ge	Diamond	5.66	−14.6	5.8	13.8
GaAs	Zinc-blend	5.65	−14.6	5.8	13.8
CdTe*	Zinc-blend	6.48	–	5.0	–

* = for reference.