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The effect of high temperatures on the electrical characteristics of Au/n-GaAs Schottky diodes

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ABSTRACT

In this study, the current–voltage *(I–V)* and capacitance–voltage *(C–V)* characteristics of Au/n-GaAs Schottky diodes have been measured over a wide temperature range, 80–480 K. The diodes were rectifying throughout the range and showed good thermal stability. Room temperature values for the ideality factor, *I–V* barrier height and *C–V* barrier height were found to be $n=1.10$, $\phi_{IV}=0.85$ eV and $\phi_{CV}=0.96$ eV, respectively. ϕ_{IV} increases and n decreases with an increase in temperature. We investigated the effect of elevated temperatures on the barrier height and ideality factor by measuring the diodes at a high temperature (annealing mode) then immediately afterwards measuring at room temperature (post annealing mode). The measurements indicate *I–V* characteristics that degrade permanently above 300 K. Permanent changes to the *C–V* characteristics were observed only above 400 K. We also noted a discrepancy in the *C–V* barrier height and carrier concentration between 340 and 400 K, which we attribute to the influence of the EL2 defect (positioned 0.83 eV below the conduction band minima) on the free carrier density. Consequently, we were able to fit the ϕ_{CV} versus temperature curve into two regions with temperature coefficients -6.9×10^{-4} eV/K and -2.2×10^{-4} eV/K above and below 400 K.

1. Introduction

Gallium Arsenide is a very important direct bandgap semiconductor. At present it is used for many applications such as solar cells in space, sources and detectors in optical fibres and as microwave sources [1–3]. The high electron mobility and high carrier saturation velocity of the material makes it ideally suited for the fabrication of high frequency and low power devices [4]. Several opto-electronic devices have been implemented on it to date. These include multi junction photovoltaics, MOSFETs and low noise avalanche photodiodes [5,6]. More often these devices require metallization, therefore in order to understand their electrical characteristics we use the simple metal semiconductor (MS) structure also known as the Schottky barrier diode [4].

The quality of a Schottky contact is notably determined by the quality of the interface between the deposited metal and the semiconductor surface [7]. In GaAs-based devices the performance has been experimentally shown to be affected to a greater extent by surface and interface defect density and also the series resistance [8]. According to Tung [9,10] it can also be explained in the chemical bonding picture, where the diode characteristics depend on the atomic structure of the MS interface.

Several researchers have studied the electrical characteristics of Au/n-GaAs Schottky diodes and have reported a strong dependence of diode characteristics on temperature [4,7,8,11–13]. Kim et al. [14] studied the temperature dependence of Au/n-GaAs *I–V* characteristics using a semi analytical model in the 83–323 K temperature range. They reported that the variations in the characteristics with temperature were consistent with those of the energy band gap. Örzeli et al. [12] explained the temperature dependence of the *I–V* and *C–V* characteristics at high temperatures (280–415 K) of Au/n-GaAs Schottky diodes using a Gaussian distribution of the Schottky barrier height. Similar experiments have been undertaken with samples exposed to and measured at the same high temperatures in other materials [15,16]. It is also important to take note of any changes and modifications as they occur when the device is exposed to high temperatures during measurement or operation since diode electrical characteristics are sensitive to heat treatment [17]. The annealing behaviour of GaAs Schottky diodes has already been the subject of a number of investigations [18–21]. Changes brought about to the diode characteristics by thermal annealing have variously been attributed to solid-phase reactions, dispersion of native oxides and failure of diffusion barriers at the interface [21,22].

However, most of these annealing studies were done systematically by exposing the diodes to high temperatures and then

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measuring them at room temperature. There is a need to compare the measurements done during annealing and post annealing. This is because, as the temperature increases, the diodes are annealed and interfacial reactions may ensue. After exposure to these high temperatures the devices may be operated at a different, and usually lower, temperature. Studying the behaviour of the devices during annealing and post annealing may yield insights important for packaging, temperature processing and safe temperature operating ranges for the GaAs devices.

In this study gold contacts were deposited on epitaxial n-GaAs. We investigated the effects of high temperatures by comparing the rectification properties and thermal stability of the MS contacts in two modes: during annealing and post annealing. The post annealing measurements were undertaken at 300 K. These 300 K measurements were designed to track any modification to the Au/GaAs system accompanying the annealing. We also considered and monitored the effects of the EL2 defect on the free carrier concentration and the rectification properties of our samples using Laplace deep-level transient spectroscopy (L-DLTS).

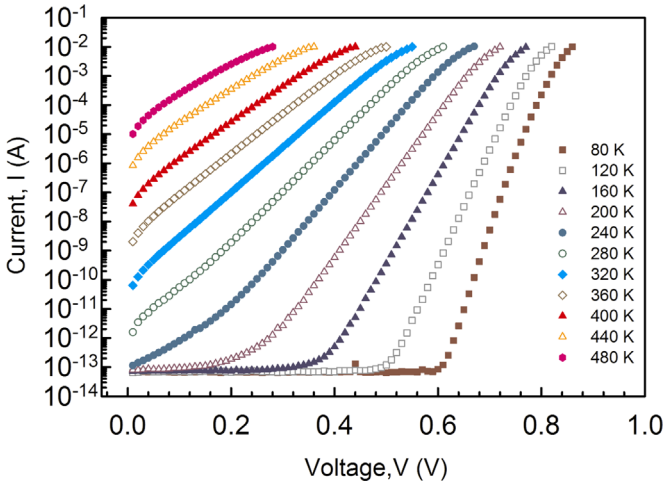

Fig. 1. Semi logarithmic forward current–voltage characteristics as a function of temperature for Au/n-GaAs Schottky diodes during annealing.

2. Experimental details

MOCVD grown n-GaAs with a free carrier density of 1.4×10^{15} cm^{-3} and $<100>$ orientation, supplied by Epi Materials Limited, was used. The wafers were first degreased by boiling in trichloroethylene for 5 min then in isopropanol for 3 min. They were then etched in a fresh solution of H_2O:H_2O_2:NH_4OH (100:1:3) for 60 s and rinsed in 18 MΩ cm deionised water. The second etching step involved removal of the native oxide layer by etching the samples in a fresh H_2O:HCl (1:1), followed by a rinse in deionised water then blow drying in compressed nitrogen gas. Au–Ge (88%:12%) ohmic contacts were evaporated on the back of the wafer in an Edwards 304 resistive coating unit pumped down to 4×10^{-7} mbar. This was followed by thermal annealing at 450 °C for 3 min in flowing argon gas.

The wafers were cleaned again, repeating the degreasing, etching and oxide removal steps. This time, an ultrasonic bath was used instead of boiling. Immediately thereafter the samples were transferred into the vacuum system for Schottky metallization. Circular contacts of 0.6 mm diameter and 500 Angstrom thickness were resistively deposited on the epitaxial layer. Temperature dependent *I–V* and *C–V* characteristics were recorded in the 80–480 K range using a JANIS closed-cycle liquid helium cryostat, an HP4140B pico-ammeter and an HP4192A LF Impedance meter. A Lakeshore 332 temperature controller with a sensitivity of ±0.1 K was used to control the temperature.

The *I–V* and *C–V* investigations were carried out in two modes: (1) during annealing, conducted at some elevated temperature in the 80–480 K range in 20 K steps, and (2) post annealing measurements, conducted at 300 K after the annealing described in (1). Once the correct annealing temperature was established, a further 5 min was allowed for the system to establish equilibrium. All the *C–V* measurements were done at 1 MHz. Finally, Laplace deep-level transient spectroscopy (L-DLTS) measurements were carried out in a JANIS cryostat within the temperature range 80–480 K.

3. Results and discussion

Our post annealing data is limited to measurements done above 300 K as no significant changes were noted for thermal treatment below 300 K. Fig. 1 shows the semi-logarithmic plot of the forward bias *I–V* characteristics of the Au/n-GaAs diodes obtained in the 80–480 K range in the annealing mode. The diodes are rectifying throughout the temperature range indicating good thermal stability. The data in Fig. 1 was fitted satisfactorily in the linear regions of the curves using the pure thermionic emission model. No well-defined linear region is observed in the 400–480 K curves. These results differ with the post annealing mode forward bias characteristics which were all fitted satisfactorily using the thermionic emission theory up to 480 K.

For pure thermionic emission, and for $(V > 3kT/q)$ the relationship between the current I and the applied bias voltage V is given by:

$$I = AA^*T^2 exp\left(-\frac{q\phi_0}{kT}\right)\left[exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

where q is the electronic charge, k the Boltzmann constant, T the absolute temperature, R_s the series resistance, ϕ_0 $(=\phi_{IV})$ the zero-bias barrier height, A the diode area and A^* $(=8.16$ A cm^{-2} K$^{-2})$ is the Richardson's constant. The prefactor of the second exponential in Eq. (1) is the reverse saturation leakage current, I_S. The ideality factor n is given by [23]:

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (2)$$

n is a measure of adherence to the pure thermionic emission theory as it reflects barrier deformation under bias [11]. The zero bias barrier height, (ϕ_0) is obtained from the reverse saturation leakage current (I_S):

$$\phi_0 = \frac{kT}{q}\ln\frac{AA^*T^2}{I_s} \quad (3)$$

A plot of variation of n and ϕ_0 against temperature during annealing is shown in Fig. 2. ϕ_0 varies from 0.78 eV at 80 K to a maximum of 0.86 eV at 400 K where as n decreases from 1.21 at 80 K to 1.02 at 400 K. This behaviour of the barrier height during annealing is contrary to the negative temperature coefficient for n-GaAs and has been observed by other researchers [7,8,23,24]. The variation of diode characteristics confirms the linear correlation between n and ϕ_0 [25].

In both modes n and ϕ_0 show a strong dependence on temperature. The dependency on temperature of diode *I–V* characteristics has been accounted for as due to several factors, chief amongst them the local non-uniformities of the Schottky barrier. At high temperatures, there are possible inhomogeneities in the interface layer thickness and non-uniformities of the interfacial charges [26]. Other authors have attributed these to changes in