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Analysis of device parameters for Au/tin oxide/n-Si(1 0 0) metal–oxide–semiconductor (MOS) diodes

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ABSTRACT

In present paper, the device parameters of tin oxide/n-Si(1 0 0) structure have been determined by means of capacitance–voltage (C–V) and conductance–voltage (G–V) measurements between 500 Hz and 1 MHz and current–voltage (I–V) measurements between −2 and +3 V at 300 K. This device has denoted good rectifying behavior and the I–V data could be described by thermionic emission (TE) technique. The values of ideality factor (n) and barrier height (Φ_B) for the sample have been determined to be 3.724 and 0.624 eV, respectively. The measured values of capacitance and conductance for the series resistance under all the biases have been corrected influence to calculate the real values of capacitance and conductance. The frequency dependence of the capacitance may be attributed to trapping states. Interface trap states of the MOS device increased by decreasing the frequency and were calculated as 1.12×10^{11} and 6.62×10^{11} $eV^{-1}\,cm^{-2}$ for 1 MHz and 100 kHz, respectively. Several important device parameters such as barrier height (Φ_B), fermi energy (E_F), diffusion voltage (V_D), donor carrier concentration (N_D) and space charge layer width (W_D) for the device have been obtained between 100 kHz and 1 MHz.

1. Introduction

Transparent conducting oxides (TCOs) films such as SnO_2, In_2O_3 and ZnO are one of the the most important materials in optoelectronic device applications, such as solar cell [1], touch screens [2], organic light emitting device (OLED) [3], diode [4] and gas sensor [5] owing to high optical transmittance in the visible region and high electric conductivity [6]. Tin oxides (SnO_2) are more chemically stable among TCOs. Tin oxide thin films have wide band gap between 3.6 and 3.9 eV relate to an n-type semiconductor [7]. For fabrication of tin oxide film a number of methods have been reported such as spray deposition [4,8], chemical vapor deposition [9], sol–gel [10], pulse laser deposition [11] and sputtering [12]. Spray deposition is a key method [13] due to its simplicity and economy with the advantage to prepare films at ambient atmosphere.

The metal–semiconductor (MS) structures are key materials for the electronic applications based on semiconductor [14–22]. The presence of tin-oxide thin layer transforms the MS to a metal/oxide/semiconductor (MOS) structure [23–25] and probable will have a prominent effect on the characteristics of diode. This oxide layer play an major role in the investigation of the device parameters [23–25]. Analysis of the I–V characteristics of the metal/semiconductor structures based on TE mechanism have shown an increase of ideality factor (n) particularly in the existence of oxide layer [23–27]. The C–V and G–V measurements ensures major information not only on the interface between dielectric film and semiconductor [28,29] for example, the density of states of interface traps [30], but also about the semiconductor layer, for example, bulk mobility and doping density [28]. The states of interface traps generally cause a frequency dispersion and bias shift of the C–V and G–V plots [31,32]. The frequency dependence of the capacitance can be referred to trapping centres of majority carriers and relaxation processes of these traps existing in the depleted region [33]. Therefore, the frequency dependent of C–V and G–V plots are major important to obtain correct and trustworthy results. Cowley and Sze [34] have made the initial works on the insulator layer between semiconductor and metal. Nicollian and Goetzberger [35] have analyzed the capacitance and conductance characteristics of the MOS device. The MOS devices create like capacitor, which accumulates the electric charge because of the dielectric feature of oxide layers. Therefore, it is important to study the change in the electrical curves at MOS devices.

In present work, spray deposition technique was used to deposit SnO_2 on n-Si(1 0 0). The goal of this work is to study the presence of SnO_2 material for electronic devices and determine the electrical properties of Au/tin oxide/n-Si(1 0 0) MOS device by means of C–V, G–V and I–V measurements at room temperature.

2. Experimental procedure

The n-type (Phosphorus-doped) Si(1 0 0) wafer have a 20 Ω cm resistivity and 380 μm thickness. The wafer has been first cleaned in methanol and acetone using ultrasonic agitation for 3 min and

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rinsed in de-ionized water (18 M Ω) and then chemically etched in a sequence of sulfuric acid+hydrogen peroxide (1:1) for 5 min, ammonia+hydrogen peroxide (1:1) for 5 min, nitric acid+hydroflouric acid+acetic acid (2:1:1) for 5 min, hydrofloric acid+de-ionized (DI) water (1:15) for 3 min. The ohmic contact was deposited by forming aluminium (Al) metal on the non-glossy surface of the n-Si wafer, then was annealed at 400 °C for 3 min. The native oxide was removed in a hydrofloric acid+DI water (1:10) and consequently, the substrate was rinsed in DI water for 3 min. Tin oxide (SnO_2) thin film was deposited on n-Si(1 0 0) substrate by spray coating a solution consisting of 27.44 wt% of stannic chloride ($SnCl_4 \cdot 5H_2O$), 40.35 wt% of DI water and 32.21 wt% of ethyl alcohol onto n-Si(1 0 0) at 450 °C. The experimental apparatus has been utilized in Ref. [8]. The gold (Au) thin film were used as dots with a diameter of approximately 2 mm on n-Si(1 0 0) substrate for Schottky contacts. The thicknesses of the aluminium ohmic and gold rectifying contact are 200 nm. All evaporation processes were performed at 4×10^{-6} Torr. The capacitance and conductance measurements were obtained between 500 Hz and 1 MHz by using LF impedance analyzer (HP 4192A). The *I–V* measurements have been obtained using a 2410 SourceMeter. All measurements carried out at 300 K.

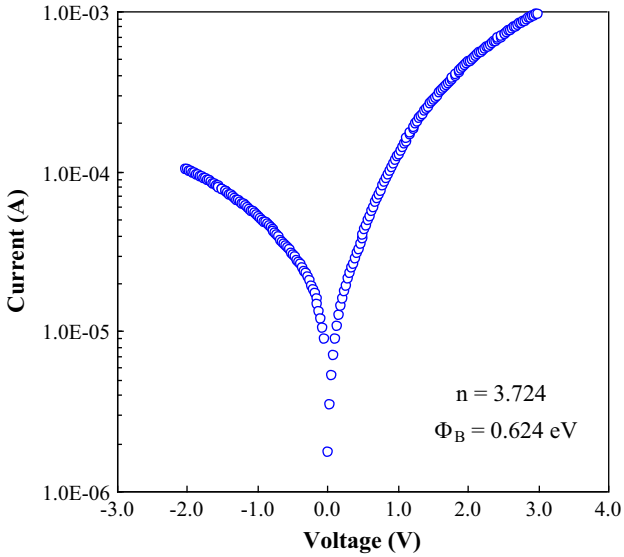

Fig. 1. The current–voltage characteristics of the Au/tin oxide/n-Si(1 0 0) MOS device.

3. Results and discussion

3.1. Current–voltage characteristics of the MOS device

The current–voltage (*I–V*) characteristics were used to calculate the device parameters. For a Schottky diode for $V > 3kT/q\infty$, The *I–V* plots were investigated according to the thermoionic emission theory by the relations [14,15]

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right]; \quad I_0 = SA^*T^2\exp\left(-\frac{q\Phi_B}{kT}\right) \tag{1}$$

where n is the diode ideality factor, I_0 is the saturation current, q is the electronic charge, Φ_B is the barrier height, A^* is the effective Richardson constant, S is the Schottky contact area, T is the absolute temperature. The experimental values of the n and Φ_B can be obtained from slopes and intercepts of the forward-bias ln I versus voltage (V) plot, respectively, as [14,15]:

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln I}\right) \text{ and } \Phi_B = \frac{kT}{q}\ln\left(\frac{SA^*T^2}{I_0}\right) \tag{2}$$

Fig. 1 represents the semilog *I–V* characteristics of the Au/tin oxide/n-Si(1 0 0) MOS device at 300 K. As shown in Fig. 1, the MOS device has rectifying behavior. The values of the n and Φ_B have been calculated from the forward semilog *I–V* characteristics using Eq. (2), respectively and given in Fig. 1. The values of the n and Φ_B of the MOS device have obtained as 3.724 and 0.624 eV, respectively. High n values can be referred to the existence of the SnO_2 layer and barrier inhomogeneities [23–27]. Many attempts in order to calculated the values of n and Φ_B of the MOS devices have been performed [23–27]. Karadeniz et al. [23] have determined 2.48 and 0.524 eV for the Al/SnO_2/p-Si(1 1 1) MOS device for values of n and Φ_B, respectively. Tuğluoğlu et al. [36] have recently obtained a n value of 4.89 with $\Phi_B = 0.679$ eV for PMI/n-Si device. Güzeldir et al. [37] calculated the n and Φ_B values of 1.73 and 0.789 eV for CdS/n-Si heterojunction, respectively. Aydoğan et al. [27] reported the values of Φ_B and n of 0.59 eV and 1.21, respectively for Au/ZnO/n-Si MOS diode.

3.2. $C-V$ and $G-V$ characteristics of the device

Fig. 2(a) and (b) depict the $C-V$ and $G-V$ characteristics for Au/tin oxide/n-Si(1 1 0) MOS device between 30 kHz and 1 MHz and at 300 K. The applied voltage range was taken between −2 and +2 V. According to Fig. 1(a) and (b), the device curves have accumulation, depletion and inversion region for all the frequency and dependent on voltage and frequency. The shape of the $C-V$ curves under for each frequency indicates n-type behaviour [14]. The capacitance values are calculated to be increase with decreasing the measured frequency, but decrease with decreasing voltage. The voltage and frequency dependencies are because of the particular features of Schottky barrier, high series resistance and impurity level [38].

The series resistance (R_s) is one of the significant parameter which induces the electrical characteristics of Schottky structures to be non-ideal [4,39]. The series resistance of MOS devices can be obtained by Nicollian and Goetzberger method [39]. From the capacitance and conductance values according to the applied voltage, the R_s can be determined through relation [4,39]

$$R_s = \frac{G_m}{G_m^2 + (\omega C_m)^2} \tag{3}$$

where G_m and C_m are the measured conductance and capaitance, respectively. Fig. 3 shows the voltage dependence of the R_s for the MOS device between 30 kHz and 1 MHz. As shown in Fig. 3, the R_s is independent of voltage at accumulation region and positive bias. The values of the R_s of MOS device at accumulation region have been determined and shown as a variation of frequency in Fig. 4. It is shown in Fig. 4 that the R_s values decrease by increasing frequency in the frequency range of 500 Hz–1 MHz, vary from 3175 Ω to 124 Ω. R_s must be considered in obtaining the voltage and frequency dependent characteristics of device.

The values of capacitance (C_c) and conductance (G_c) corrected according to the values of the series resistance obtained between 30 kHz and 1 MHz are determined by using the following relations [4,40]

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{a^2 + \omega^2 C_m^2}, \quad G_c = \frac{(G_m^2 + \omega^2 C_m^2)a}{a^2 + \omega^2 C_m^2}$$
$$a = G_m - (G_m^2 + \omega^2 C_m^2)R_s \tag{4}$$

The voltage dependence of the C_c and G_c characteristics for Au/tin oxide/n-Si(1 0 0) MOS device between 100 kHz and 1 MHz is plotted in Fig. 5(a) and (b) from Eq. (4). As seen in from Figs. 2 and 5(a), the values of capacitance increased after correction the series resistance (R_s). The tin oxide layer capacitance (C_{ox})