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Silicon epitaxy on textured double layer porous silicon by LPCVD

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ABSTRACT

Epitaxial silicon thin film on textured double layer porous silicon (DLPS) was demonstrated. The textured DLPS was formed by electrochemical etching using two different current densities on the silicon wafer that are randomly textured with upright pyramids. Silicon thin films were then grown on the annealed DLPS, using low-pressure chemical vapor deposition (LPCVD). The reflectance of the DLPS and the grown silicon thin films were studied by a spectrophotometer. The crystallinity and topography of the grown silicon thin films were studied by Raman spectroscopy and SEM. The reflectance results show that the reflectance of the silicon wafer decreases from 24.7% to 11.7% after texturing, and after the deposition of silicon thin film the surface reflectance is about 13.8%. SEM images show that the epitaxial silicon film on textured DLPS exhibits random pyramids. The Raman spectrum peaks near 521 cm^{-1} have a width of 7.8 cm^{-1}, which reveals the high crystalline quality of the silicon epitaxy.

1. Introduction

The high cost of solar modules restricts the widespread use of photovoltaics. About half of the price of photovoltaic silicon modules is due to the silicon wafers and over 90% of the solar cells are made from crystalline silicon wafers [1]. Therefore, reduction of silicon material consumption is at the moment urgently required. A thin film monocrystalline silicon solar cell without the need for slicing and with high conversion efficiency reduces the material consumption to below 1 g Si per watt [2]. For this goal, different methods are proposed. Direct deposition on foreign substrate is still limited now by low growth rate or contamination from the substrate [3]. The transfer of monocrystalline silicon films onto various types of foreign substrates such as plastics is a promising and successful way of fabricating thin and flexible monocrystalline silicon devices [4,5]. The transfer layer process is based on the formation of a high-quality substrate for epitaxial silicon deposition, which could be re-used several times [2]. In layer transfer processes DLPS is formed by electrochemical anodisation in hydrofluoric acid (HF) containing electrolyte. During subsequent high temperature annealing [6], the surface of the upper layer closes together and forms quasi-monocrystlline silicon (QMS) layer, which serves as a seeding layer for epitaxial growth. While the bottom layer permits easy removal of the epilayer from the substrate by application of mechanical force, transfer of the porous films onto a foreign substrate can be obtained either before or after device fabrication as proposed in the literature.

Because of the low optical absorption, efficient light trapping schemes are necessary for thin film crystalline silicon solar cells. Surface texture has been usually formed after epitaxy, which will sacrifice a certain amount of epitaxial silicon. A very promising approach is to grow epitaxial layers by chemical vapor deposition (CVD) on a textured wafer that has porous silicon at the surface. After epitaxy, the textured epitaxial layer can be separated from the substrate wafer by applying mechanical stress to the sintered porous silicon (SPS) [7].

In this paper, we focused on the realization of DLPS on a pre-textured silicon wafer and subsequent LPCVD epitaxy. Epitaxial growth on conventional DLPS and on pre-textured DLPS was compared and discussed.

2. Experimental details

The silicon substrates used were (1 0 0)-oriented, Czochralski-grown p-type silicon wafers with a resistivity of 0.01–0.02 Ω cm. Firstly, the silicon wafers were immersed in a 25% NaOH solution at 85 °C for 5 min to remove the surface damaged layer. After being cleaned by deionized water and dried by blowing Ar over the wafers, the samples were textured with randomly positioned upright pyramids by immersing in a mixture of 2.5% NaOH (quality proportion) and 5% isopropylalcohol (IPA) (volumetric proportion) at 80 °C for 40 min. Then DLPS samples were prepared by electrochemical etching on the textured silicon wafers. For comparison we also prepared DLPS samples on planar silicon

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wafers. The electrolyte consists of a mixture of hydrofluoric acid and ethanol in a volumetric proportion of 1:1. Etching solution is diluted with ethanol for good surface wetting, which improves pore uniformity [6]. Porosity depends on the type of silicon, orientation and doping level and also on the anodisation parameters such as currnet density and HF concentration. Thickness of DLPS depends on anodisation time, current density and HF concentration [5]. In this study, the current density for the low porosity layer and the high porosity layer are 7 and 200 mA/cm^2, respectively. The anodisation time is set at 50 s for the first current density and at 25 s for the second current density. The porosity obtained is approximately 20% on the surface and 50% on the underlayer, which was obtained from the average of at least four samples.

The samples were annealed in hydrogen atmosphere at 1100 °C for 30 min. After the annealing, the upper low porous layer resulted in a monocrystalline surface, the so-called quasi monocrystalline silicon (QMS) layer, and the high porous layer yielded large cavities and thus transformed into a mechanically weak layer. Then, high-temperature chemical vapor epitaxy from SiH_4 was used to produce a monocrystalline silicon film on the recrystallized layer. The chamber was pumped down to a base pressure of about 3×10^{-4} Pa. At the same time, the chamber heating began. The ramp rate was adjusted typically at 10 °C/min. Once the temperature reached 1100 °C, SiH_4 was introduced into the chamber, and pressure was kept below 100 Pa. After the deposition was finished, the gas flow was stopped, and the chamber was evacuated.

Structural properties and evolution after thermal annealing of the DLPS were investigated by SEM (LEO-1530VP). The crystallinity and topography of the grown silicon thin films were monitored by SEM and Raman spectroscopy (Raman T64000). The Raman spectra were taken at room temperature using excitation light from an argon ion laser (514.5 nm). A 180° reflective optical geometry was used for data collection. The resolution was 0.5 cm^{-1}. The reflectance of samples was investigated by a UV–vis–NIR Spectrophotometer (Cary 5000).

3. Results and discussion

The starting silicon wafer was first randomly textured with upright pyramids by immersion of the silicon wafer in NaOH solution. Fig. 1 shows SEM micrographs of the textured surface. We can see that almost all the top surface is covered by pyramidal textures.

The reflectance in the visible regions of the starting silicon wafer, the silicon wafer after the removal of surface damaged layer and the textured silicon wafer were investigated. The spectra are shown in Fig. 2. It can be seen that the lowest reflectance of the starting silicon wafer is about 23%, and the value increased to about 31% after removing the surface damaged layer. This is because the starting silicon surface is rough, but after the removal of the surface damaged layer the silicon surface becomes relatively flat, so that reflectance increases. Calculated in the range of 400–800 nm, the average reflectances of the three samples were 24.7%, 34.3% and 11.7%. It is evident that the reflectance reduced greatly after texturing. This is mainly due to the enhanced path length of the incident light in the film.

DLPS was then typically formed on the pre-textured silicon wafer using two different current densities. DLPS on planar silicon wafers was also prepared. The porosity of the top low porosity layer is in the range of 10–20% and the porosity of the below high porosity layer is in the range of 50–70%. The low porosity at the surface eases the closure of the pores while the high porosity of the separation layer eases the separation of the epitaxial film from the growth substrate [8]. Fig. 3 shows the top porous surface of DLPS formed on (a) pre-textured silicon wafer and (b) planar silicon wafer in the as etched state. Cross-sectional views are shown as insets in Fig. 3. In order to show more clearly, a partial view is also shown as an inset in Fig. 3(a). Comparing Fig. 3(a) and Fig. 1, it can be seen that the formation of DLPS does not destroy the pyramid structure of the surface. However, due to the pyramid structure it is difficult to observe the upper nano-pores. From Fig. 3(b), it can be seen that the structure size of the upper nano-pores is only about 30 nm. The distribution of the pores is irregular. From the cross-sectional view we can clearly see a high porosity layer beneath the low porosity layer. The low porosity upper layer has a sponge-like structure, while the high porosity lower layer has a branched structure.

Fig. 4 shows the important structural change that occurs at the top surface of the low porosity layer of DLPS formed on (a) pre-textured silicon wafer and (b) planar silicon wafer after thermal annealing under hydrogen atmosphere at 1050 °C for 30 min. It is observed from Fig. 4(a) that the shape of the top surface changes from upright pyramids to the cell shape. It was also observed from Fig. 4(b) that the top porous and spongy-like surface is transformed into an almost pore free and smooth surface. This

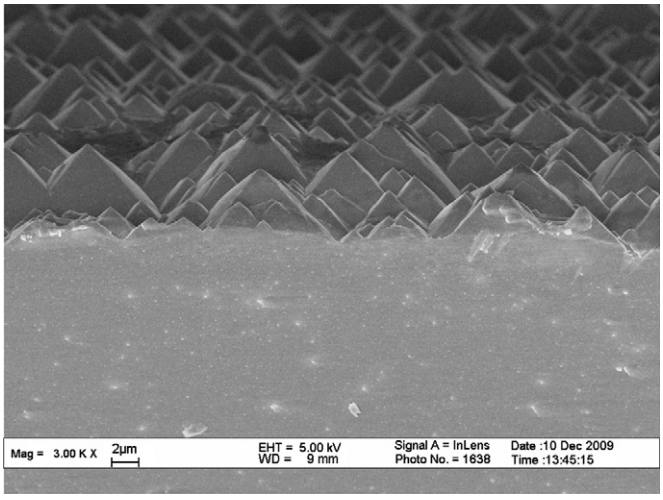

Fig. 1. Cross-sectional SEM image of the textured silicon wafer.

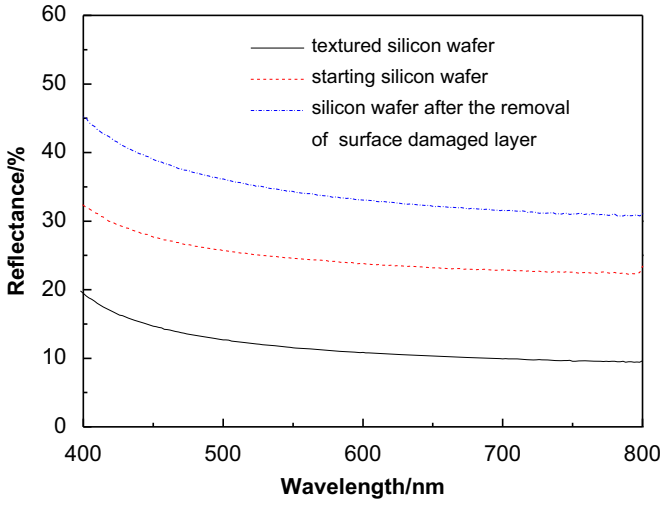

Fig. 2. Reflectance of the starting silicon wafer, the silicon wafer after the removal of surface damages layer and the textured silicon wafer.