Available online at www.sciencedirect.com
ScienceDirect
Physica B 403 (2008) 2690–2697
PHYSICA B
www.elsevier.com/locate/physb

Investigation of diode parameters using I–V and C–V characteristics of In/SiO_2/p-Si (MIS) Schottky diodes

Ö.F. Yüksel[a,*], A.B. Selçuk[b], S.B. Ocak[b]

[a]*Department of Physics, Faculty of Arts and Science, Selçuk University, Kampus, Konya 42075 Turkey*
[b]*PK, 14 Etlik, Ankara, Turkey*

Received 5 January 2007; received in revised form 29 January 2008; accepted 29 January 2008

Abstract

A study on interface states density distribution and characteristic parameters of the In/SiO_2/p-Si (MIS) capacitor has been made. The thickness of the SiO_2 film obtained from the measurement of the corrected capacitance in the strong accumulation region for MIS Schottky diodes was 220 Å. The diode parameters from the forward bias I–V characteristics such as ideality factor, series resistance and barrier heights were found to be 1.75, 106–112 Ω and 0.592 eV, respectively. The energy distribution of the interface state density D_{it} was determined from the forward bias I–V characteristics by taking into account the bias dependence of the effective barrier height. The interface state density obtained using the I–V characteristics had an exponential growth, with bias towards the top of the valance band, from $9.44\times10^{13}\,eV^{-1}\,cm^{-2}$ in 0.329-E_v eV to $1.11\times10^{13}\,eV^{-1}\,cm^{-2}$ in 0.527-E_v eV at room temperature. Furthermore, the values of interface state density D_{it} obtained by the Hill–Coleman method from the C–V characteristics range from 52.9×10^{13} to $1.11\times10^{13}\,eV^{-1}\,cm^{-2}$ at a frequency range of 30kHz–1 MHz. These values of D_{it} and R_s were responsible for the non-ideal behaviour of I–V and C–V characteristics.

Keywords: MIS Schottky diodes; Insulator layer; I–V; C–V; Frequency dependence; Series resistance; Interface state density

1. Introduction

The metal–semiconductor (MS) contact is one of the most widely used rectifying contacts in device technology [1–4]. It is well known that, unless specially fabricated, a Schottky barrier diode possesses a thin interfacial native oxide layer between the metal and the semiconductor. The existence of such an interfacial insulator layer converts the device to a metal–insulator–semiconductor (MIS) diode [5–18] and may have a strong influence on the diode characteristics as well as a change of the interface state charge with bias, which may give rise to an additional field in the interfacial layer [10]. The performance and reliability of Schottky diode is drastically influenced by the interface quality between the metal and semiconductor surface [10]. Therefore, it is important to determine the interface properties of a Schottky diode. The existence of such an insulating layer can have a strong influence on the diode characteristics as well as an the interface state density, ideality factor and barrier height. Furthermore, the forward bias current–voltage (I–V) characteristics are linear in the semilogarithmic scale at low voltages but deviate considerably from linearity due to the effect of the parameters, such as the series resistance (R_s), the interfacial layer and the interface states when the applied voltage is sufficiently large [10–18]. Interface states at the Si–SiO_2 interface have been studied in detail because of their effects on the reliability and quality of MIS diodes [10–16]. The popularity of such studies comes from their importance in the semiconductor industry.

The characterisation of the interface states in Schottky barrier diodes is determined by capacitance and conductance–frequency techniques, which are extensively used for electrical characteristics. A study (of the alternating current (ac) conductance of MIS capacitors) made by Nicollian and Goetzberger [7] indicated that conductance measurement can be used to distinguish the effects of trapping at

*Corresponding author.
E-mail address: fyuksel@selcuk.edu.tr (O.F. Yüksel).

0921-4526/$ - see front matter © 2008 Elsevier B.V. All rights reserved.
doi:10.1016/j.physb.2008.01.039

the interfacial insulator layer-semiconductor interface. They have observed that the capacitance decreases with increasing frequencies. These effects are obtained at low and intermediate frequency capacitance–voltage (C–V) and G–V measurements. Interface states can affect the C–V characteristics of MIS structures, causing a bending of the $1/C^2-V$ as well as increasing the ideality factor. In general, a C–V plot shows an increase in capacitance with an increase in forward bias. There are several possible sources of error that cause deviations of the ideal behaviour, such as electrical properties and must be taken into account. These properties include the effects of the insulator layer between the metal and the semiconductor; interface state density (D_{it}), series resistance (R_s) and formation of barrier height (Φ_B).

Various measurement techniques for determining interface state density have been developed, and among them the important one is the Hill–Coleman technique [19]. This technique is a powerful tool to deduce interface state density and has been used by some authors [20–22]. The forward bias C–V and G–V measurements give important information about the density or energy distribution of the interface states of the structure. In general, the C–V and G–V plots in the ideal case are frequency independent [7–16]. However, this ideal case is often disturbed due to the presence of an interfacial layer between the contact materials and interface states at the interfacial layer–semiconductor interface [10–22]. Therefore, the frequency-dependent electrical characteristics are very important to obtain accurate and reliable results. Chattopadhyay and co-workers [14,15] studied the capacitance of Schottky barrier diodes and observed an anomalous peak in the forward bias C–V characteristics, and also investigated the C–V characteristics of Schottky barrier diodes considering the series resistance effect. The model proposed in Ref. [15], however, investigates only the C–V plot in the high-frequency limit when interface states cannot follow the a.c. signal.

In this paper, we have investigated the characteristic parameters obtained from the experimental forward bias current voltage (I–V) and reverse bias capacitance voltage (C–V) of In/SiO_2/p-Si (MIS) Schottky barrier diodes. We measured the C–V and $G/\omega-V$ characteristics for a wide frequency range (30 kHz–1 MHz) at room temperature in dark, and also reported a systematic investigation on the frequency dependence of the interface states density and series resistance from capacitance and conductance characteristics in In/SiO_2/p-Si (MIS) structures. To determine the accurate values of R_s and D_{it}, we applied the method by Nicollian and Goetzberger [5,7] and Hill–Coleman [19], respectively. Experimental results show that both D_{it} and R_s are important parameters that influence the electrical characteristics of Schottky barrier diodes with thin interfacial layer.

2. Experimental procedure

The semiconductor substrates used in this work were p-type B-doped Si single crystals with a (1 0 0) surface orientation, 280 μm thick and 0.8 Ω cm resistivity. Before making contacts, the Si wafer was degreased for 5 min in boiling trichloroethylene, acetone and ethanol, consecutively. The wafer was chemically cleaned using the RCA cleaning procedure (i.e., a 10 min boil in $NH_3+H_2O_2+6H_2O$, followed by a 10 min boil in $HCl+H_2O_2+6H_2O$) with the final dip in diluted HF for 30 s, and then rinsed in deionized water of resistivity 18.3 MΩ cm with ultrasonic vibration and dried by high-purity nitrogen. Immediately after surface cleaning, high-purity aluminium (Al) metal (99.999%) with a thickness of 1500 Å was thermally evaporated from the tungsten filament onto the whole of the back surface of the wafer about 2×10^{-6} Torr. Then, a low-resistivity ohmic contact was followed by a temperature treatment at 500 °C for 3 min in N_2 atmosphere. After the ohmic contact was made, the front surface of the Si wafer was exposed to air in a clean glass box for 1 month at room temperature to native oxidation. The Schottky contacts were formed on the other faces by evaporating indium (In, 99.999%) with a thickness of 1500 Å as dots with a diameter of about 1.0 mm through a metal shadow mask in the pressure of 2×10^{-6} Torr. Metal layer thickness as well as deposition rates were monitored with the help of a digital quartz crystal thickness monitor (FTM6). The deposition rates were about 10–20 Å s^{-1}. Ten dots (Schottky contact) on the same semiconductor surface were performed for the In/SiO_2/p-Si (MIS) Schottky barrier diodes (Fig. 1). The variation of calculated parameters is almost the same with each other. We have introduced only one diode in this paper. The interfacial layer thickness was estimated to be about 220 Å from the measurement of the corrected capacitance in the strong accumulation region at 1 MHz for the MIS Schottky diode [10].

The I–V measurements were performed using a Keithley 220 programmable constant current source, a Keithley 614 electrometer. The capacitance–voltage (C–V) and conductance–voltage ($G/\omega-V$) measurements were performed at various frequencies using an HP 4192A LF impedance analyzer at room temperature in dark at a test signal of 40 mV_{rms} [10].

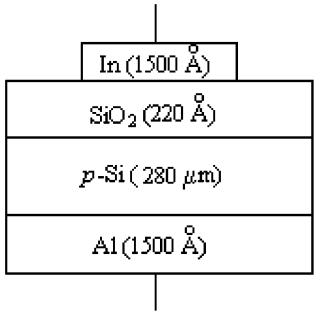

Fig. 1. Cross-sectional view of In/SiO_2/p-Si Schottky diode.