Physica B 404 (2009) 1494–1497

Contents lists available at ScienceDirect

Physica B

journal homepage: www.elsevier.com/locate/physb

Annealing temperature effect on electrical characteristics of Co/p-type Si Schottky barrier diodes

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ARTICLE INFO

Article history:
Received 22 January 2008
Received in revised form
26 December 2008
Accepted 6 January 2009

PACS:
73.30.+y
73.40.Sx
73.40.Ei
73.40.Ns

Keywords:
Annealing temperature
Silicon
Barrier heights
Ideality factor

ABSTRACT

The electrical characteristics of Co/p-type Si Schottky barrier diodes (SBDs), which were formed at various annealing temperatures from 200 to 600 °C, were investigated using current–voltage (*I–V*) techniques. The Schottky barrier height at 200 °C annealing temperature was found to be 0.708 eV (*I–V*). However, the Schottky barrier height of the Co/p-type Si diode slightly decreases to 0.696 eV (*I–V*) when the diode was annealed at 300 °C for 5 min in N_2 atmosphere. It is noted that the Schottky barrier height increased to 0.765 eV at 400 °C, 0.830 eV at 500 °C and 0.836 eV at 600 °C for 5 min in N_2 atmosphere. This increase was attributed to that the annealing removes the passivation effect of the native oxide layer and reactivates the surface defects which are responsible for the Fermi level pinning. Norde method was also used to extract the barrier height of Co/p-type Si Schottky barrier diodes and the values are 0.704 eV for the 200 °C, 0.714 eV at 300 °C, 0.80447 eV at 400 °C, 0.874 eV at 500 °C and 0.874 eV at 600 °C which are in good agreement with those obtained by the *I–V* method.

1. Introduction

Metal–semiconductor (MS) contacts are frequently used in integrated circuits, e.g. as gates in MESFETs or MOSFET, in light detectors and as solar cells. Early X-ray photoemission spectroscopy (XRPS) measurements showed that ideal clean surfaces of III–V semiconductors exhibited no intrinsic surfaces states in the energy gap to pin the Fermi level. That is, Fermi level is not pinned at the free clean surface these semiconductor. However, the defect model predicts that Fermi level pinning will occur on a real surface as a result of extrinsic surface states induced by a metal or oxide layer [1–8]. The performance and stability of MS structures is of vital importance to all electronic and optoelectronics devices [1–13]. As will be discussed below, many researches have attempted to understand the physical parameters of Schottky barrier diodes (SBD). However, the fundamental physical mechanisms that determine SBD parameters such as ideality factor n and the barrier height (BH) Φ_b are still not fully understood. The popularity of such studies, which is rooted in their importance to the semiconductor industry, does not assure uniformity of the results or of interpretation. SBDs are among the simplest MS contact devices [14–17]. Schottky diodes (SDs) with low BH have found applications in devices operating at cryogenic temperatures as infrared detectors and sensors in thermal imaging [18–20].

The thermal annealing behaviour of SBDs is of wide interest for scientific as well as technological reasons [2,21]. Inter-diffusion, contaminations, chemical reaction, compound formation, interface roughening, defect generation, dopant migration, a flat diode interface, etc. can all derive by thermodynamics due to the thermal annealing [21–23]. The conventional contacts preparation by deposition of metallic films on the Si can suffer from problems arising from the presence of a native oxide and surface defects at metal–Si interface [21–24]. Such a contact is generally unstable because of the tendency for inter-diffusion and compound formation at the interface in the device preparation and performance [21–24]. Furthermore, the chemical reactions between the metal and semiconductor due to thermal annealing can cause inter-diffusion of the elements at the interface. It is well known that various detrimental defects could be introduced during heat treatments. These are well documented in low-resistivity Si, however, less is known of the effect annealing has on the electrical properties of highly resistive p-type Si [25,26]. Therefore, analysis of the current–voltage (*I–V*) characteristics of the SBDs at room temperature only does not give detailed

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doi:10.1016/j.physb.2009.01.010

information about their conduction process or the nature of barrier formation at the MS SDs. The formation of more reliable and thermally stable Schottky contacts is essential for the application of power amplifiers and optoelectronic devices operating at high temperatures.

Many researches have attempted to understand the electrical characteristics of SBD [27–32]. For example, Reddy et al. [28] were reported on the electrical and structural properties of Ru/Au Schottky contacts on n-GaAs as function of temperature in the range of annealing temperatures 400–600 °C. Ayyildiz et al. [29] have examined the effects of the interface state on the non-ideal *I–V* characteristics of the SDs annealed from 200 to 400 °C with steps of 100 °C. Ramesh et al. [30] have examined ideality factor and SBHs by *I–V* measurements as a function of annealing temperature. Nuhoğlu et al. [31] have presented relations between the experiment BH and equilibrium interface charge density, interface charge density distribution curves from the *I–V* characteristics of the SBD, depending on annealing temperature. Sha et al. [32] were reported the effect of annealing on the interface state density distribution of Ni–silicided Si_{1-x} Ge_x SDs from *I–V* and *C–V* characteristics. The most important feature characterizing a SBD is its BH. In spite of the numerous applications of Schottky barriers, the factors controlling the BH are not completely understood [14–17]. Among the different methods available for metallization of Si surfaces, vacuum deposition is the usual metallization method, and electrodeposition also is an interesting method due to its valuable advantages such as the possibility of metal deposition at low temperature with low costs.

In the present study, we have investigated relations between the experiment BHs and ideality factor from current–voltage measurements of the Co/p-type Si SBD prepared by electrodeposition method, depending on annealing temperature. The electrodeposition of Co films on p-type Si substrate has been carried out at a constant current density from an aqueous electrolyte of sulfate of Co. These SBD were annealed at temperatures from 200 to 600 °C with steps of 100 °C.

2. Experimental procedure

The used p-type Si wafer was (1 0 0) oriented and with free carrier concentration of $2.25\times10^{15}\,cm^{-3}$ from the reverse bias C^{-2}-*V* characteristics at room temperature (at 300 K). The wafers were chemically cleaned using the RCA cleaning procedure [5,13,20]. The RCA cleaning procedure is the industry standard for removing contaminants from wafers. The RCA cleaning procedure has three major steps used sequentially: (i) organic clean: removal of insoluble organic contaminants with a 5:1:1 H_2O:H_2O_2:NH_4OH solution, (ii) oxide strip: removal of a thin silicon dioxide layer where metallic contaminants may accumulated as a result of (i), using a diluted 50:1 H_2O:HF solution, and (iii) ionic clean: removal of ionic and heavy metal atomic contaminants using a solution of 6:1:1 H_2O:H_2O_2:HCl. The procedure was also designed to prevent replanting of metal contaminants from solution back to the wafer's surface. When finished, the polished side should be seculars with no residue.

The native oxide on the front surface of the substrates was removed in HF:H_2O(1:10) solution and finally, the wafer was rinsed in de-ionized water for 30 s. Then, low resistivity ohmic back contact to p-type Si (1 0 0) wafer was made by using Al, followed by a temperature treatment at 570 °C for 3 min in N_2 atmosphere. The Schottky contacts were formed on the front face of the *p*-Si as dots with diameter of about 1 mm (diode area $=7.85\times10^{-3}\,cm^2$) by the galvanostatic electrodeposition of Co. Acid resistant adhesive tape was used to mask off all the substrate except for the deposition area. The electrodeposition of Co films on p-type Si substrate has been carried out at room temperature from an aqueous electrolyte containing 1 M Co sulphate and 0.5 M boric acid. The *p*-Si substrate was used as cathode while a Pt plate was anode. A current density of 3 mA/cm^2 was maintained between the two electrodes. Film thickness was determined as 150 nm by deposition time. The current–voltage (*I–V*) characteristics were measured using a Keithley 487 Picoammeter/Voltage Source at room temperature and in the dark.

3. Results and discussion

The current–voltage (*I–V*) characteristics of Co/p-type Si SBD measured as a function of annealing temperature are shown in Fig. 1. As can be seen from Fig. 1, the properties of all Co/p-type Si SBD are uniform over different diodes. The reverse bias saturation current was about 8.17×10^{-8} A at 0.0 V for the 200 °C, whereas for the samples annealed at 300, 400, 500 and 600 °C diode saturation current values are 6.69×10^{-8}, 7.95×10^{-9}, 5.33×10^{-9} and 4.63×10^{-9} A at −0.0 V, respectively.

When a SBD is considered, it is assumed that thermionic emission current for charge transport under the forward bias can be expressed as [2]

$$I = I_0\,\exp\left(\frac{qV}{nkT}\right)\left[1-\exp\left(-\frac{qV}{kT}\right)\right] \tag{1}$$

with

$$I_0 = AA^*T^2\exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{2}$$

where I_0 is the saturation current density, Φ_{b0} is the zero bias effective SBH, A^* is the effective Richardson constant and equals to 32 A/cm^2 K^2 for p-type Si [2,5,13]; *A* the diode area, *n* is an ideality

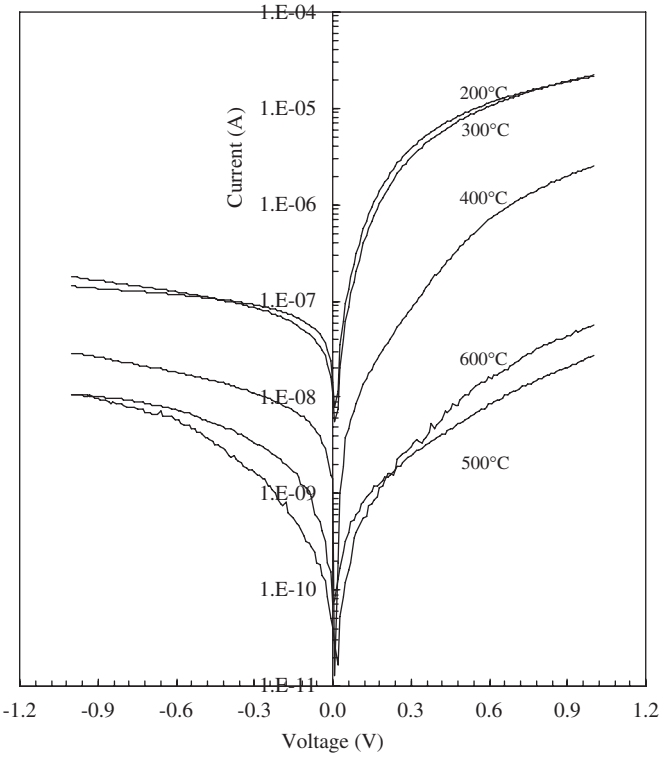

Fig. 1. Experimental forward and reverse bias current versus voltage characteristics for the Co/p-type Si Schottky diode as a function of annealing temperature.