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Electronic states at misfit dislocations in partially relaxed InGaAs/GaAs heterostructures

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Abstract

Electronic properties of strain-induced dislocations in partially relaxed InGaAs/GaAs heterostructures with a small lattice mismatch have been studied by means of deep-level transient spectroscopy (DLTS). DLTS investigations carried out with Schottky contacts revealed one deep electron trap, at about E_C−0.57 eV. The trap has been attributed to electron states associated with α misfit dislocations lying at the interface between the epilayer and the substrate. Thorough studies including DLTS-line shape, DLTS-line behaviour analysis as well as capture kinetics and deep profile measurements made possible to specify the type of electronic states associated with dislocations. We relate the electron trap to "localized" states at misfit dislocations.
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1. Introduction

Lattice-mismatched InGaAs/GaAs heterostructures are of a continual scientific interest, not only from their potential technological application in high-speed and optoelectronic devices, but also because of being very instructive for understanding the dislocation-related relaxation processes. Furthermore, the heterostructures with a small lattice mismatch exemplify an excellent semiconductor material for studying deep electronic states at dislocations. Strain relaxation unlike plastic deformation does not introduce, except dislocations, a large amount of point defects in the crystal, which are known to strongly contribute to the investigated electronic properties of extended defects [1,2]. In such heterostructures, due to the difference in lattice parameters between the epitaxial layer and the substrate, a stabile elastic strain is relieved by the formation of misfit dislocations at the interface provided that the thickness of the epilayer exceeds a certain critical value. Misfit dislocations are accompanied by threading dislocations, which propagate into the epitaxial layer. Both kinds of dislocations are known to introduce deep-lying energy levels in the form of one-dimensional (1D) bands in the band gap, acting as recombination centres or traps for free carriers.

The experimental studies of electronic properties of spatially extended defects usually involve the application of various electrical and optical techniques, such as deep-level transient spectroscopy (DLTS), electron beam induced current (EBIC), photoluminescence (PL), etc. Nowadays, the DLTS [3] is one of the most powerful techniques widely used for studying electronic properties of deep-level defects in semiconductors. It is a well-elaborated tool for investigating deep point-defect levels, whereas in the case of extended defects, the observed DLTS-line features are usually far from simple interpretation and need much careful analysis [4]. Several problems have to be taken into account when studying spatially extended, many-electron defects, namely a time-dependent electrostatic potential barrier built up at the dislocation during the filling process, and limiting the successive charge capture [5], which manifests itself in DLTS as the so-called "logarithmic filling law" or as non-exponential capacitance transients

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resulting in broadened DLTS peaks [1,4,6]. These anomalous features are currently considered as "fingerprints" of dislocations in semiconductors, provided that the other specific phenomena like high trap concentration as compared to the shallow level doping [7], strong electric-field influence on the trap emission [8] or alloy composition fluctuations in compound semiconductors [9,10] can be excluded.

Over the last two decades, attempts to analyse the DLTS signal coming from dislocations in different semiconductor materials have been undertaken by many authors [1–6,9–16]. An enormous contribution to this point was made by Schröter and co-workers [6,13–16]. They showed that the electronic states associated with extended defects in semiconductors can be classified as "localized" or "bandlike" by taking into consideration the rate R_i at which the states attain their internal electron equilibrium [14]. A comparison of the internal equilibration rate with the carrier emission rate R_e and the carrier capture rate R_c of the defect, necessary to attain the equilibrium with conduction and valence bands, makes it possible to distinguish between "localized" ($R_i \ll R_e, R_c$) and "bandlike" ($R_i \gg R_e, R_c$) density of states. By means of computer simulations of DLTS spectra, the authors demonstrated that these two types of states can be distinguished on the basis of the DLTS-line variation with the filling-pulse time [14,15].

In our recent paper [17], we have extensively discussed some peculiar features of DLTS signals originating from deep-level traps, associated with both point and extended defects in semiconductor materials. We concluded that the application of a set of specific criteria containing DLTS-line shape, DLTS-line behaviour analysis and capture kinetics measurements, makes possible to distinguish between these two classes of defects and to determine the type of their electronic states. In this communication, we report DLTS studies of electrical properties of stress-induced dislocations in partially relaxed InGaAs/GaAs heterostructures with a small lattice mismatch. A detailed analysis of DLTS-signal features in the case of a dislocation-related trap made possible to specify the type of its electronic states as well.

2. Experiment

The samples were $In_xGa_{1-x}As$ films epitaxially grown on the GaAs substrates by metalorganic vapour-phase epitaxy (MOVPE) technique. A growth was performed with the use of atmospheric pressure MOVPE system, fitted with an AIX-200 R&D horizontal reactor made by AIXTRON. The organometallic group III sources were TMGa (trimethylgallium) and TMIn (trimethylindium) and were transported by passing H_2 through bubblers. AsH_3 was used as the arsenic source reactant. The structure consisted of a (0 0 1)-oriented n^+-GaAs substrate, a 0.5 μm thick and Si doped n-GaAs buffer layer with a net donor concentration $2 \times 10^{17}\,cm^{-3}$, and of about 160 nm thickness $In_xGa_{1-x}As$ epitaxial layer with background doping concentration at about $10^{16}\,cm^{-3}$. All the epitaxial layers were grown at the same temperature equal to 670 °C.

The composition of the epitaxial layer was deduced from high-resolution X-ray diffraction rocking curve measurements. The structural analysis indicated that the sample was partially relaxed. The calculated indium content of the $In_xGa_{1-x}As$ epitaxial layer was 7.7% corresponding to the difference in the lattice parameter between GaAs and the ternary compound of about 0.55%. It should result in a generation of 2D network of 60° misfit dislocations lying along two orthogonal $\langle 1\,1\,0 \rangle$ crystallographic directions at the (0 0 1) interface [18,19].

The electrical characteristics were measured for the Schottky diodes deposited in vacuum by evaporation of a $0.44\,mm^2$ circular Au layer, by standard lift-off technique on the front side of the sample. Prior to the Schottky contacts formation, the ohmic contacts were prepared on the backside of the n^+-GaAs substrate by Au/Ge alloy evaporation, and annealing was carried out in 600 °C for several seconds. The quality of the Schottky barrier was checked up by the I–V–T and C–V–T measurements, indicating good rectifying characteristics. The barrier height Φ_B of the sample was determined as 0.7 eV, and the ideality factor and the series resistance were found to be equal to about 1.1 and 1 Ω, respectively, remaining almost invariant in the range of the measured temperatures.

All the deep-level spectra were taken using the DLTS technique within the 200–400 K temperature range with the help of a DLS-82E spectrometer manufactured by Semitrap (Hungary), based on a 1 MHz capacitance bridge and a lock-in type integrator [20]. The double-correlation DLTS (DDLTS) method with two filling pulses, U_1 and U_2, of different heights and the same width was applied [21]. This way, the measurement conditions could be selected to ensure that the observed DLTS signal comes from the narrow layer of the depletion region including the interface between the epitaxial layer and the substrate, where misfit dislocations should be generated.

3. DLTS results

The DLTS analysis of deep-level defects in partially relaxed $In_{0.077}Ga_{0.923}As$/GaAs heterostructures has been made using the Schottky barrier diodes formed onto the epitaxial layers. It allowed us to investigate only the majority electron carriers in the upper half of the band gap.

The one deep electron trap labelled E1 has been revealed by means of DDLTS under bias conditions chosen as follows. The probed region included the interface between the epilayer and the substrate, i.e. under a quiescent reverse voltage $U_R = -1\,V$ and two filling pulses, $U_1 = 0\,V$ and $U_2 = -0.5\,V$, respectively. The width of the pulses was equal to 20 μs. Exemplary DLTS spectra for several different lock-in frequencies, i.e. different thermal emission rates, are given in Fig. 1. The activation energy, i.e. energy level position (E_C–E_T) and the capture cross-section (σ_n)

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