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Leakage current in Ti/4H-SiC Schottky barrier diode

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Abstract

The Ti/4H-SiC Schottky barrier diodes with an edge termination structure are fabricated. The low on-resistance of $3\,\mathrm{m\Omega\,cm^2}$ and low-leakage current of $10^{-2}-10^{-4}\,\mathrm{A/cm^2}$ over 1500 V are obtained. Current–voltage characteristics are evaluated by device simulation considering metal–semiconductor interface conditions such as bunching steps and interface pinning traps. Device simulation suggests that the variation of barrier height originated from the variation of interface pinning-trap concentration influences on the leakage current. Bunching steps have an effect on the leakage current because the electric field is enhanced at the bottom of the bunching steps.

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Keywords: SiC power device; The Schottky barrier; Interface pinning; Bunching steps

1. Introduction

Wide band gap semiconductor materials having high breakdown electric field are needed for high-power semiconductor devices. The breakdown electric field in SiC, 3 MV/cm, is one order of magnitude higher than that in Si. Hence, the SiC Schottky barrier diode (SBD) is expected to have better steady loss and switching loss, compared to Si pin diode [1]. We have already reported fabrication of Ti/4H-SiC SBDs without any intentional edge termination and those properties, Schottky barrier height of 1.0–1.2 eV, breakdown voltage of 1500 V and on-resistance (differential resistance) of $3\,\mathrm{m\Omega\,cm^2}$ [2,3]. The measured Schottky barrier height is higher than the value estimated from work function of the electrode metal, Ti. The measured leakage current and breakdown voltage are close to the calculated value, in the device simulation considering pinning at metal/semiconductor (M/S) interface, which brings higher Schottky barrier height [2–4].

In order to reproducibly obtain the breakdown voltage close to the material limit, edge termination structure such as the guard ring is preferable. In this paper, SBDs with the guard ring structure are fabricated and characterized. The guard ring structure is fabricated by ion implantation and activation anneal. Bunching steps appear in SiC surfaces after annealing process. Similar to SBDs without intentional edge termination, low specific on-resistance and high breakdown voltage are attained in SBDs with the guard ring structure. In addition to the interface pinning trap, influence of surface conditions such as bunching steps on SBD characteristics is investigated.

2. Fabrication and measurement

The structure of a fabricated SBD device is shown in Fig. 1. 4H-SiC wafers with n-type drift layer epitaxially grown on an n-type substrate were employed. The nominal doping concentration and thickness of drift layer were $5\times10^{15}\,\mathrm{cm^{-3}}$ and 10 μm, respectively. The guard ring structure, selectively formed p-type region around the Schottky contact, was employed for the edge termination structure, and was fabricated by ion implantation of Al and subsequent activation anneal in Ar ambient around 1400 °C. Bunching steps with 10–30 nm height and 0.21 μm interval appeared after activation anneal over 1400 °C, because wafers have (0 0 0 1) face with 8° off towards ⟨1 1 −2 0⟩ orientation for poly-type control. Ni sputtering and rapid thermal annealing were used for

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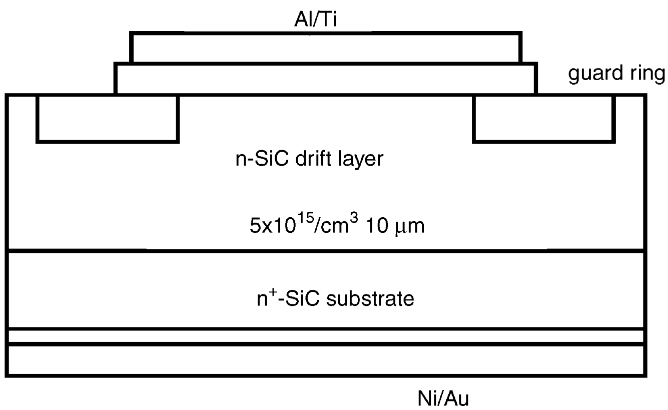

Fig. 1. Device structure of fabricated Ti/4H-SiC SBD.

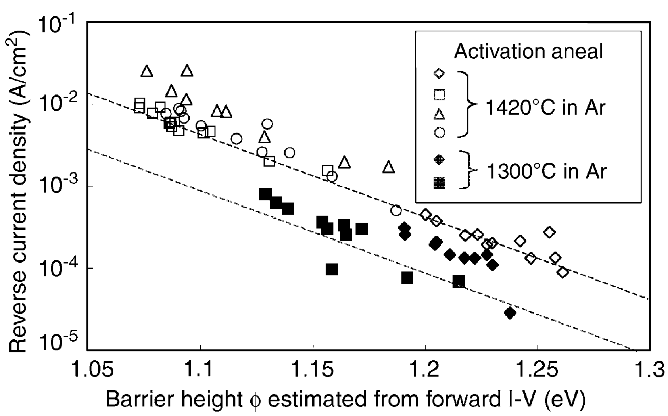

Fig. 2. Relation between barrier height ϕ measured from forward I–V characteristics and leakage current in Ti/4H-SiC SBD.

formation of n-type back contact. Ti sputtering was employed for formation of the Schottky electrode. The Schottky electrodes with 500 μm diameter were fabricated by wet etching of Ti. Anode and cathode electrodes are metallized by Al and Au, respectively.

Forward current–voltage (I–V) characteristics show ideality factor, n, of 1.01–1.02 and low on-resistance of 3 mΩ cm^2. Reverse I–V characteristics show relatively high breakdown voltage over 1500 V. The obtained on-resistance and breakdown voltage are close to the theoretical limit estimated from breakdown electric field of SiC. These values are comparable to those in SBD without intentional edge termination structures [2,3]. The Schottky barrier height is evaluated from forward I–V characteristics. Measured barrier height ϕ is 1.07–1.27 eV, which is relatively high compared to the estimated value from work function of Ti, 0.6–0.7 eV [4], and is close to the value estimated from hybrid orbital reference energy level for surface pinning [5] and band offset of 4H-SiC [6]. Higher barrier height is considered to be due to Fermi level pinning at M/S interface. One of the possible origins of the pinning is an electron trap induced by sputtering process of the Schottky electrode.

Fig. 2 shows the relation between barrier height ϕ estimated from forward I–V characteristics and leakage current in reverse I–V characteristics. It is revealed that the leakage current decreases with the increase of barrier height ϕ. For the 0.1 eV change of barrier height ϕ, the leakage current changes by one order of magnitude. SBDs with little bunching steps, which are annealed at 1300 °C, show lower leakage current than the SBDs with bunching steps, annealed at 1420 °C for the same barrier height ϕ. The leakage current in SBDs with bunching steps is five times larger than that with relatively flat surface. The influence of barrier height, pinning trap concentration, and bunching steps on device properties is discussed by using device simulation.

3. Device simulation

Synopsys technology-computer-aided-design (TCAD) is used for device simulator to calculate I–V curves. Employed impact ionization coefficients are values reported by Konstantinov et al. [7]. Barrier tunneling effective mass is 0.66, which is effective density mass employed in TCAD. A high-resistivity thin layer with thickness of 5 nm is used for description of pinning at M/S interface in TCAD. Barrier height at M/S interface, M/S barrier height, is set to 0.6–0.7 eV, which is close to the value estimated from work function of Ti. Traps in the high-resistivity layer are assumed to be deep acceptors with a capture cross-section σ of 10^{-14} cm^{-2} and activation energy E_t of 0.5 eV. These trap parameters have been evaluated in the previously reported analysis [3]. Electric field enhancement at the Schottky electrode edge is minimized by the interface pinning trap in these trap parameters, and the experimental results that the breakdown voltage close to the material limit is obtained even in SBDs without intentional edge termination are explained. Trap density is set to fit the measured forward I–V characteristics. The calculation is semi-quantitative, because the exact value of barrier tunneling mass and the detailed concentration profile of the pinning trap near the interface have not been identified.

Fig. 3(a) shows the calculated reverse I–V characteristics for SBDs with barrier height ϕ of 1.2 eV. Schematic illustration of devices with and without bunching steps is shown in Fig. 3(b). The interval of bunching steps was 0.21 μm. The leakage current in SBDs with bunching steps is larger than those without bunching steps. The electric field at M/S interface at 1200 V is 1.66 MV/cm in SBDs with a flat surface (without bunching steps). The electric field in SBDs with bunching steps increases to 1.9 MV/cm at the bottom region of bunching steps. Larger electric field in SBDs with bunching steps increases leakage current due to Schottky barrier tunneling. The increase in the calculated leakage current is consistent with the measured results.

In SBDs with bunching steps, the calculated reverse characteristics for the change of barrier height of 0.1 eV