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Design and test of component circuits of an integrated quantum voltage noise source for Johnson noise thermometry

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ABSTRACT

We present design and testing of a pseudo-random number generator (PRNG) and a variable pulse number multiplier (VPNM) which are digital circuit subsystems in an integrated quantum voltage noise source for Jonson noise thermometry. Well-defined, calculable pseudo-random patterns of single flux quantum pulses are synthesized with the PRNG and multiplied digitally with the VPNM. The circuit implementation on rapid single flux quantum technology required practical circuit scales and bias currents, 279 junctions and 33 mA for the PRNG, and 1677 junctions and 218 mA for the VPNM. We confirmed the circuit operation with sufficiently wide margins, 80–120%, with respect to the designed bias currents.

1. Introduction

Johnson noise thermometry (JNT), based on the Johnson–Nyquist noise of a resistor [1], is one of the promising types of primary thermometry. The sense probe is similar to those used for a resistance thermometer in size and structure. It is applicable to a wide temperature range of 50–1400 K, an important feature for systematic temperature measurements [2].

The uncertainty of the JNT measurement has been greatly reduced for the past ten years. One of the reasons is introduction of a quantum voltage noise source (QVNS) as a reference, based on a technique to synthesize a quantum-accurate and calculable waveform using a pulse-driven Josephson junction (JJ) array [3–5]. On the other hand, high-frequency control instruments are required to drive the JJ array, which increases system complexity, cost and electromagnetic interference (EMI). Also, it takes a lot of time to calculate digital codes for synthesizing pseudo noise waveforms.

To overcome the problems, we previously proposed an integrated QVNS (IQVNS) [6]. The concept is to integrate control functions into a rapid single flux quantum (RSFQ) chip in combination with a voltage multiplier (VM) used for an RSFQ digital-to-analog converter [7]. It is expected to reduce system complexity, cost and EMI.

Previously, we created an IQVNS model, and broke down it into component-level specifications [6]. The component circuits were optimized for the measurement of the noise of a 100-ohm resistance temperature detector (RTD) at the temperature of the triple point of water (TPW), 273.16 K, whose power spectrum density (PSD) is 1.51 nV^2/Hz.

In this paper we describe design and test of digital circuit components of the IQVNS optimized for the measurement of the noise of the 100-ohm RTD at the temperature of the TPW.

2. Circuit design

2.1. IQVNS model

The IQVNS has five parameters (m, f_{clk}, τ, N_1 and N_2) characterizing the pseudo noise and comprises three components: a pseudo-random number generator (PRNG) [8], a variable pulse number multiplier (VPNM) [9,10] and a voltage multiplier (VM) [11]. The PRNG produces an m-bit maximum-length-sequence (MLS) at a clock frequency of f_{clk}. The VPNM multiplies the number of single flux quantum (SFQ) pulses produced by the PRNG by a factor N_1 with a pulse repetition interval of τ. The VM multiplies the number of SFQ pulses from the VPNM by a factor N_2.

By using Eqs. (1) and (2) in Ref. [6], the IQVNS PSD for an SFQ-pulse shape approximated by a rectangle with a width τ_{SFQ} and a height Φ_0/τ_{SFQ} is given by

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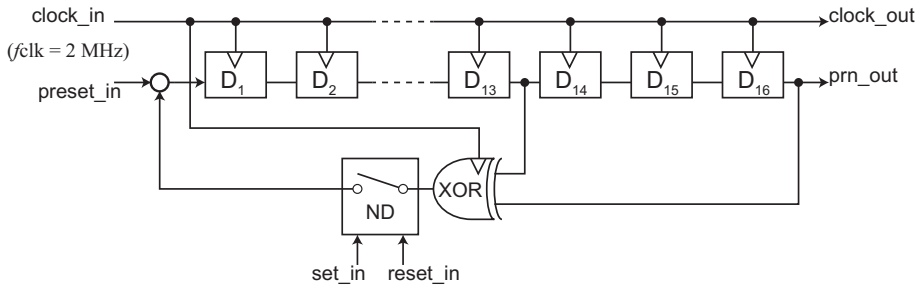

Fig. 1. A block diagram of the PRNG for the 17-bit MLS. The circuit comprises a 16-stage SR, an XOR gate and an NDRO gate. "D" and "ND" denote a delay flip-flop and an NDRO gate, respectively.

$$PSD_{IQ}(f) = \frac{2\Phi_0^2 f_{clk}}{1-2^{-m}} \frac{\sin^2(\pi N_1 f\tau)}{\sin^2(\pi f\tau)} N_2^2 \mathrm{sinc}^2(\pi f \tau_{SFQ}), \quad (1)$$

where $\Phi_0 = 2.07 \times 10^{-15}$ Wb is the SFQ and $\mathrm{sinc}(x) = \sin(x)/x$ is a sampling function. The spectrum expressed by Eq. (1), though slightly dependent on frequency, is highly calculable for the accurate JNT measurements [6]. We can choose a practical set of the parameters for JNT at the TPW corresponding to $PSD_{IQ}(0) \sim 1.51$ nV^2/Hz, for example, which is yielded by $m = 17$, $f_{clk} = 2.013$ MHz, $\tau = 200$ ps, $N_1 = 74$ and $N_2 = 4$. Eq. (1) also shows that the frequency dependence becomes weaker with decreasing τ or τ_{SFQ}, suggesting possible improvement by design optimization for high speed operation or by technology development for high-Jc and small-area junctions.

To date, the design technique of the VM has been basically matured [11]. In this section we focus on design of the PRNG and VPNM with the above-mentioned five parameters. We used the CONNECT cell library for circuit design [12].

2.2. PRNG

Fig. 1 shows a block diagram of the PRNG with parameters $m = 17$ and $f_{clk} = 2.013$ MHz. For 17-bit MLS generation, the PRNG comprises a 16-stage feedback shift-register (SR) and an exclusive OR (XOR) gate. We should note that the RSFQ XOR gate has a delay of 1 clock period. We employed a nondestructive read-out (NDRO) gate as a switch in the feedback line after the XOR, which enables all the SR bits to be zero states by resetting the NDRO followed by applying 16 clock pulses. After presetting of the SR, the PRNG produces the MLS synchronized with the clock signal. The PRNG is made up of 279 JJs with a dc bias current of 33 mA.

The spectrum of the MLS pseudo random noise is discrete because of the finite code length $M = 2^m - 1$. The tone interval f_{clk}/M should be as narrow as a frequency resolution of the JNT system for achieving high measurement accuracy. Our JNT system operates at $f_{clk} \sim 2$ MHz and has a frequency resolution of 1 Hz [5] so that $M \sim 2 \times 10^6 (m = 21)$ is a desirable number at which the spectrum is considered as practically continuous similar to actual Johnson noise. The circuit modification can be easily done by adding 4 SR stages to the current design.

2.3. VPNM

Fig. 2 shows a block diagram of the 8-bit VPNM with a variable multiplication factor N_1 ranging from 1 to 255. By combining the VM with a fixed multiplication factor of $N_2 = 4$, the total multiplication factor N_1N_2 ranges from 4 to 1020. The N_1N_2 range covers $PSD_{IQ}(0)$ of 2.8×10^{-4} nV^2/Hz to 18 nV^2/Hz, which corresponds to a PSD range with a 100-ohm RTD at 50 mK to 3200 K. The VPNM

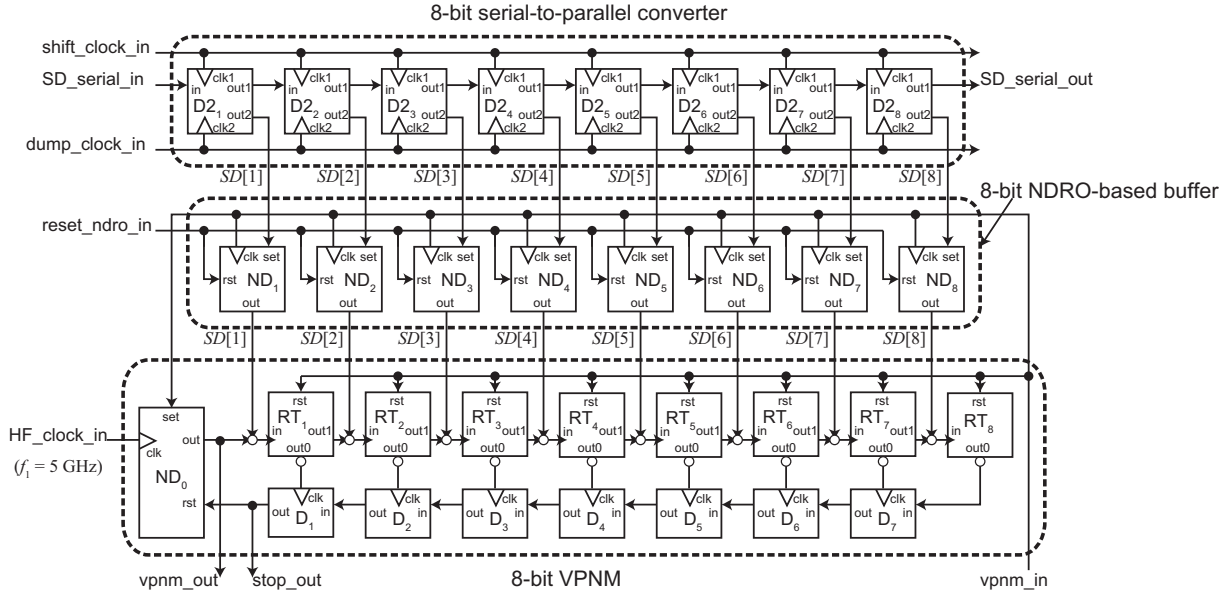

Fig. 2. A block diagram of the 8-bit VPNM in combination with the 8-bit serial-to-parallel converter and the 8-bit NDRO-based buffer. The VPNM comprises the 8-bit variable counter and an NDRO gate. "D", "D2", "ND" and "RT" denote a delay flip-flop, a double delay flip-flop, an NDRO gate and a resettable toggle flip-flop, respectively.