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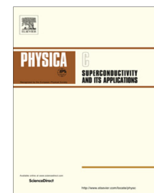

Heat transfer analysis of a programmable Josephson voltage standard chip operated with a mechanical cooler

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ABSTRACT

We are developing a 10 V programmable Josephson voltage standard (PJVS) system using a 10 K mechanical cooler that enables liquid-helium-free operation. In our previous experiments, we identified a problem that the optimum bias operating points may be affected by the heating effect of the chip depending on the output voltage. In this study, we have observed cross-sectional and in-plane structures of the PJVS chip module in order to determine the cause of the heating effect. We perform a heat transfer analysis using the finite element method with several models based on the observation results. We confirm a temperature increase of approximately 100 mK at the chip surface, due mainly to unintended voids in the InSn solder.

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1. Introduction

The programmable Josephson voltage standard (PJVS) is a very promising standard that is currently being widely researched worldwide. It is among several new types of Josephson voltage standards, and was proposed by Hamilton et al. in 1995 [1]. The output voltage of the PJVS can be programmed to have arbitrary values by controlling the ON/OFF states of the bias current applied to each segment, enabling us to realize a digital-to-analog (D/A) converter operation with a quantum–mechanical-theory-based accuracy. To realize more user-friendly and low operating-cost systems, a liquid-helium-free PJVS system using a mechanical refrigerator has been developed at the National Institute of Advanced Industrial Science and Technology (AIST) [2].

Recently, we successfully generated DC and AC voltage signals that were greater than 10 V using PJVS systems [3,4]. At AIST, we are now attempting to include one of the systems in the national standard for DC voltages, which is currently being realized using a conventional liquid-helium-based system. However, in the 10 V voltage generation experiments of the PJVS system, we identified a problem wherein the optimum operating bias points may shift depending on the output voltage [3]. From the initial values that were independently optimized for each segment, the observed bias shift corresponding to the 10 V output was found to be approximately 0.15 mA. One of the possible reasons for the bias shift in our system is believed to be the heating effect in the chip because the chip is not entirely cooled using liquid helium, but is cooled only from its bottom using a mechanical cooler. Assuming the heating effect, the observed bias shift corresponds to the temperature rise of approximately 100 mK. In this study, we first attempted to observe the actual structure of the PJVS chip module in order to investigate the source of the heating effect. We observed many unintended voids in the InSn solder layer between the Si chip and the sapphire substrate. We then examined the cross-sectional and in-plane temperature distributions in the chip module by performing heat transfer analysis using the finite element method based on several models corresponding to the observed structures in the chip module. We also discuss the parameter dependences and the cases involving AC voltage generation.

2. Observation of PJVS chip module

2.1. Structure

Fig. 1a shows a schematic cross-sectional diagram of our PJVS chip module mounted on the cold stage. The PJVS chip is composed

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of a series array of 524,288 NbN-based superconductor-normal metal-superconductor (SNS) Josephson junctions [5]. The junctions are fabricated on a 15 mm × 15 mm Si chip that is bonded on a sapphire substrate using an InSn (the eutectic alloy of 52 wt% In and 48 wt% Sn) solder. The cold stage, on which the PJVS module is placed is cooled using a Gifford McMahon (GM) refrigerator, and is maintained at a temperature of around 10 K. The module include the PJVS chip, consists of 9 layers from the lowest layer near the cold stage, as shown in Fig. 1b, which are as follows (the numbers in parentheses indicate the nominal thickness of each layer) [5]: 1. In (100 μm), 2. Al_2O_3 (600 μm), 3. Au (0.1 μm), 4. InSn (10 μm), 5. Au (0.3 μm), 6. Pd (0.4 μm), 7. Si (400 μm), 8. NbN (0.3 μm) and 9. SiO_2 (0.3 μm). Layers 7–9 comprise the PJVS chip, while layers 3, 5, and 6 are the buffer layers. The junction array, which exists as a Joule heat source between layers 8 and 9, is omitted from the figure. The total heat resistance of these layers is estimated to be about 10–20 mK/W. On the other hand, the power consumption at the junction array is calculated by summing the Joule heat of (10 V × 10 mA =) 0.1 W with the applied microwave power loss of approximately 0.2 W to give 0.3 W. Therefore, the expected temperature rise is more than one order of magnitude smaller than the experimental estimation of 100 mK as mentioned in Section 1. We then attempted to observe the actual structure of our PJVS module.

2.2. Voids in InSn layer

Fig. 2a shows a cross-sectional microphotograph and its enlargements for a polished PJVS chip module. From these observations, the thickness of the InSn layer, which is located in the center of the pictures, is estimated to be approximately 8 μm (±4 μm). This value is consistent with our expected values. It is noted that there are many voids, as indicated by dark grey or black spots in the figure, in the InSn solder layer. It seems in Fig. 2a that both the surfaces of the Si and Al_2O_3 substrates, which are buffered with thin Au layers, are covered with thin InSn solder even with the voids, suggesting that the voids are not caused by the lack of wettability. In the assembly process of the module, the InSn solder is heated up to approximately 150 °C with flux for soldering. Therefore, we speculate that such the voids might be caused by bubbling of the flux and/or thermal shrink of the solder after the heating process. Though the chip modules used for the observations in this section have not experienced cryogenic temperature, thermal cycling from room temperature to an operating temperature of approximately 10 K could also have some effects for the void structure [6–9]. We need further study to clarify the cause for the voids and their stability.

In order to reveal the in-plane distribution of the voids, we then made observations of another chip module using a scanning acoustic microscope (SAM), as shown in Fig. 2b. In this figure, the white areas now represent the voids while the dark grey areas correspond to the dense solders. We observed many unintended voids in the InSn solder layer, and the area ratio of the voids is estimated to be about 80% of the in-plane area of the chip. Because the existence of such the voids might seriously affect the heat transfer in our chip module, we then evaluated the cross-sectional and in-plane temperature distribution by performing computer simulations considering the void structures.

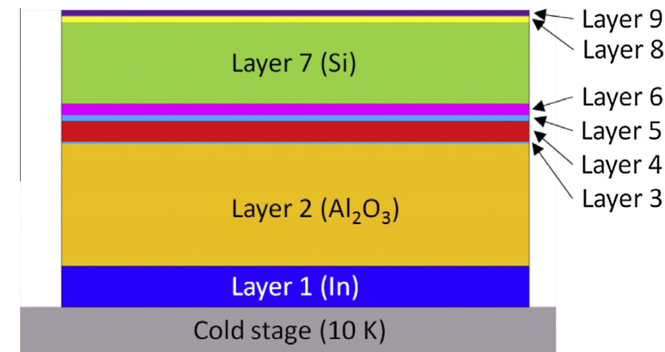

Fig. 1a. Structure of PJVS module.

3. Heat transfer analysis for DC voltage generation

3.1. Analysis method and models

We used the software tool, *ANSYS*, to carry out for the heat transfer analysis based on the finite element method. Fig. 3 shows the three-dimensional model to be analyzed with the layer structure, as shown in Fig. 1a. The heat source with a total DC power of 0.3 W is located at 2/3 of the area on the NbN layer surface because the microwave splitters without heating are placed at the other 1/3 of the area. The boundary condition at the bottom of the In layer is fixed at a nominal cold stage temperature of 10 K while the other surfaces (the top of the Si layer and the side edges) are assumed to be thermally insulated. In our calculation, we ignored the effect of thermal radiation. The thermal conductivity at 10 K in each layer was assumed as shown in the legend table in Fig. 1b. Based on the findings in Section 2.2, we employed three analysis models called the "Uniform model", the "Donut model" and the "Island model" as shown in Figs. 4a, 4b and 4c. Uniform model was assumed to be InSn layer are all uniformly soldered. Donut model and Island model was expressed for the presence of voids in the InSn layer in a donut shape and island. In Donut model's analysis, without changing the area ratio of the voids relative to that of the entire chip, we varied the number of voids to be 1, 4, 9 to make the model close to the actual structure, as shown in

Layer number	Color	Material	Thickness (μm)	Thermal conductivity (W/mK)(@10 K)	Specific heat (J/kgK)	Density (kg/m^3)
9		SiO_2	0.3	0.1	0.4	2200
8		NbN	0.3	1	0	8470
7		Si	400	2600	0.5	2329
6		Pd	0.4	1150	4	12050
5		Au	0.3	3240	2.5	19300
4		InSn	10	9	0.4	7290
3		Au	0.1	3240	2.5	19300
2		Al_2O_3	600	3000	0.4	3970
1		In	100	588	18	7280

Fig. 1b. Materials, thickness, thermal conductivity at 10 K, specific heat and density of the PJVS module.

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