



# Reduction of the jitter of single-flux-quantum time-to-digital converters for time-of-flight mass spectrometry



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## ABSTRACT

We have been developing a high-resolution superconducting time-of-flight mass spectrometry (TOF-MS) system, which utilizes a superconducting strip ion detector (SSID) and a single-flux-quantum (SFQ) time-to-digital converter (TDC). The SFQ TDC can measure time intervals between multiple input signals and directly convert them into binary data. In our previous study, 24-bit SFQ TDC with a  $3 \times 24$ -bit First-In First-Out (FIFO) buffer was designed and implemented using the AIST Nb standard process 2 (STP2), whose time resolution and dynamic range are 100 ps and 1.6 ms, respectively. In this study we reduce the jitter of the TDC by using two different approaches: one uses an on-chip clock generator with an on-chip low-pass filter for reducing the noise in the bias current, and the other uses a low-jitter external clock source at room temperature. We confirmed that the jitter is reduced to less than 100 ps in the latter approach.

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## 1. Introduction

Time-of-flight mass spectrometry (TOF-MS) is a basic analytical technique used in various fields, such as, chemistry, and medicine. Recently, ultra-fast response time of a superconductive strip ion detector (SSID) was demonstrated for the detection of biomolecules [1–3]. The SSID brings about a high mass resolution and a high count rate in the TOF-MS, which are unattainable in conventional ion detectors. However, the practical response time of the SSID is currently limited by the bandwidth of the output voltage amplifier at room temperature and long wires between the detector and the amplifier.

To solve this problem, we are developing a high-resolution time-to-digital converter (TDC) [4] using single-flux-quantum (SFQ) circuits [5], which operates at the same stage with the SSID. The SFQ TDC can measure the time intervals of multiple input pulses with the time resolution of several picoseconds, and directly convert them into binary data. Our TOF-MS system uses the matrix-assisted laser desorption ionization (MALDI) method [6]. Since tens of molecules are successively detected at one shot of laser irradiation, the SFQ TDC has to measure the multiple time intervals of successive input signals from the detector at high rate. In our TOF-MS system, the rise time of the SSID is sub-nanosecond,

therefore the time resolution of the TDC is designed to be 100 ps. Because the target measurable maximum molecular weight is 600,000 Da, the dynamic range of the TDC is set to be 1.6 ms.

In our previous study, we confirmed the correct operation of the SFQ TDC. However, the measured jitter was much larger than expected: 40 ns for the time interval of 50  $\mu$ s [4]. This was probably caused by considerably large jitter of clock signals generated by the SFQ ring oscillator. In this study, two types of SFQ TDCs are designed and implemented to reduce the jitter: one uses an on-chip clock generator with an on-chip low-pass filter for reducing the noise in the bias current, and the other uses a low-jitter external clock source at room temperature. The jitter of these TDCs are evaluated experimentally.

## 2. Design and jitter evaluation of previous SFQ TDC

In our previous study, we have designed 24-bit SFQ TDC using the AIST 2.5 kA/cm<sup>2</sup> Nb standard process (STP2) [7] and the CONNECT cell library [8]. Fig. 1 shows a block diagram of the SFQ TDC. The TDC is composed of a 10 GHz SFQ clock generator (CG) [9], a 24-bit binary counter, a  $3 \times 24$ -bit asynchronous First-In First-Out (FIFO) buffer and a 24-bit shift register (SR) for readout.

In operation, when a “start” signal is input to the SFQ TDC, SFQ pulses at 10 GHz are sent to the binary counter. When “read” signals from the SSID are detected, the data in the counter are sent to the FIFO buffer and stored there. The stored data can be read out to

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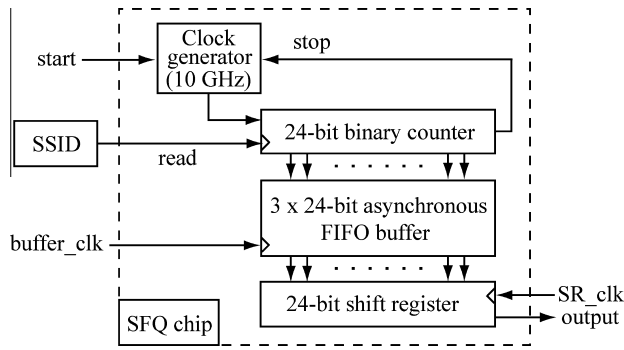


Fig. 1. Block diagram of an SFQ TDC with an on-chip SFQ CG.

the room temperature electronics by inputting a “buffer\_clk” signal and 24 “SR\_clk” signals. Finally, when the counter overflows, it sends a “stop” signal to the CG to finish the measurement, meanwhile the counter is reset. The TDC has a  $3 \times 24$ -bit FIFO buffers, therefore it can store three sequences of counted data. If the next data arrive at the FIFO buffer from the counter while three data are stored in the FIFO, the last data from the counter are simply ignored.

The operation of the TDC with an on-chip SFQ CG had been measured using the measurement setup depicted in Fig. 2. All bias currents for the SFQ chip were filtered by using first-order low-pass filters with the cut-off frequency of 16 Hz at room temperature. Input signals for the TDC were input by using data generator at room temperature. The output signals from the SFQ chip were amplified by differential amplifiers with the band width of 1 MHz. Obtained results are shown in Fig. 3 [4]. In this measurement, we measured the time intervals between “start” and “read” signals by using the TDC 1000 times and made histograms. Fig. 3(a and b) shows a histogram of measured time intervals for  $50 \mu\text{s}$  and a dependence of the full width at half maximums (FWHMs) of measured histograms on the time intervals of input pulses, respectively. Fig. 3 shows that the measured time interval is scattered significantly and the FWHMs of the peak linearly increase with the increase of the time intervals of input pulses.

We suspected that the large jitter is caused by the SFQ ring oscillator, which is used in the SFQ CG. The ring of the SFQ CG is composed of 22 Josephson junctions. When the time interval is  $50 \mu\text{s}$ , an SFQ pulse goes around the ring 500,000 times. The estimated total jitter of the SFQ CG is about 300 ps for the time interval of  $50 \mu\text{s}$  referring the jitter of the JTL reported previously [10]. The measured jitter of the TDC was larger than 100 times of the estimated jitter. Since the frequency of the SFQ ring oscillator depends on the supply current to the oscillator, the large jitter is thought to be caused by the current noise superimposed on the bias current of the ring oscillator.

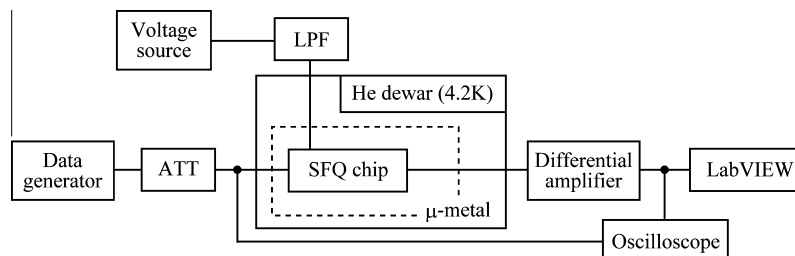


Fig. 2. Measurement setup for an SFQ TDC with an on-chip SFQ CG.

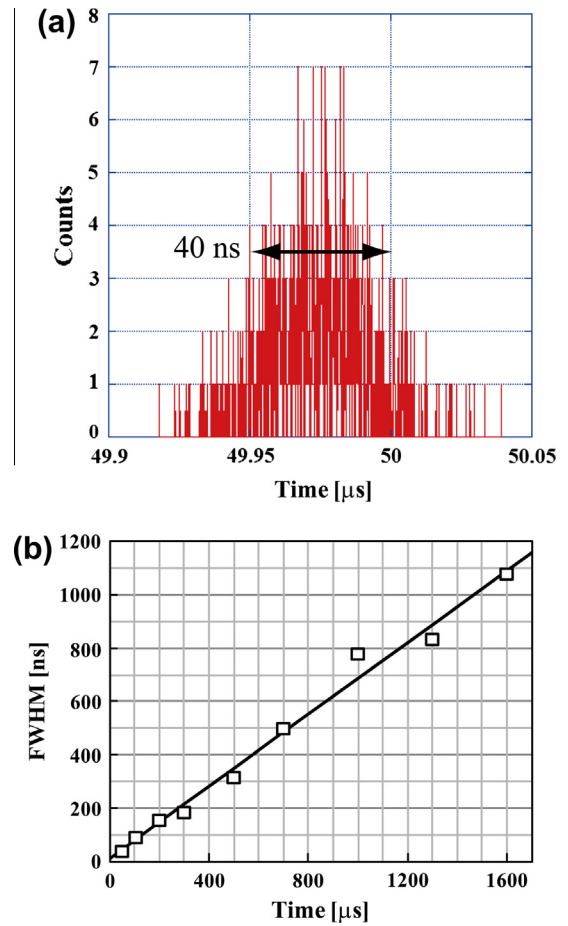


Fig. 3. Experimental results obtained in the previous SFQ TDC with an on-chip SFQ CG. (a) A histogram of the measured time interval for  $50 \mu\text{s}$ . The time resolution in the histogram is 100 ps. (b) The dependence of the FWHM of measured peaks on the time intervals of input pulses.

### 3. Designs of improved SFQ TDCs

The reduction of the jitter of the SFQ TDC was attempted by using two different approaches. In the first approach, the jitter of the on-chip SFQ CG is improved by using on-chip low-pass filter in the bias supply line. The second approach uses a low-jitter external clock source.

#### 3.1. SFQ TDC with an on-chip low-pass filter

In order to reduce the external noise in the bias supply line of the on-chip SFQ CG, an on-chip first-order low-pass filter (LPF) was added to the SFQ TDC. The LPF consists of a series resistor

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