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Yield analysis of large-scale adiabatic-quantum-flux-parametron logic: The effect of the distribution of the critical current



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ABSTRACT

We performed yield analysis of large-scale adiabatic-quantum-flux-parametron (AQFP) circuits using circuit simulations based on the Monte Carlo method assuming the distribution of the critical current of Josephson junctions. Based on the simulation results, we also made an analytical model for the circuit yield of large-scale AQFP circuits. The yield analysis indicates that AQFP integrated circuits containing 1 million gates can be realized when the interconnect inductance is about 40 pH and the normalized standard deviation of the critical current is less than 1%.

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1. Introduction

We are studying adiabatic-quantum-flux-parametron (AQFP) logic for realizing ultimately energy-efficient integrated circuits. In AQFP logic, the shape of the potential energy is adiabatically or gradually changed from a single-well potential to a double-well potential, by which the energy consumption of the logic gate can be reduced proportional to the operating frequency. We have investigated the parameter conditions for the AQFP logic gate to operate in the adiabatic mode [1,2], and verified its low-energy logic operation with 10 zJ at 5 GHz experimentally [3]. The functional operation of a 1-bit AQFP full adder has been also demonstrated [4].

The current gain of the AQFP logic gate is substantially large and infinite in the ideal case where there is no distribution in the circuit parameters and no thermal fluctuation. However the non-uniformity of the critical current of the junction pair composing the AQFP logic gate brings about the offset in the input current, resulting in the malfunction of the logic gate in an extreme case. Besides, a long interconnection between AQFP gates causes the reduction of the input current for the next AQFP gate and enlarges the possibility of the malfunction. Both these effects would be obstacles when realizing large-scale AQFP integrated circuits.

In this study, we evaluate the relationship between the circuit yield and the distribution of the critical current I_c of AQFP circuits using circuit simulations based on the Monte Carlo method [5–8]. Furthermore, we also make an analytical model for the circuit yield of large-scale AQFP circuits based on the simulation results, taking account of the distribution of the critical current and the interconnect inductance.

2. Evaluation of circuit yield using Monte Carlo method

The circuit yields of multiple stages of AQFP gates were calculated by using the Monte Carlo method, where each circuit parameter was scattered according to the Gaussian distribution function. We prepared many sets of circuit parameters for multiple stages of AQFP gates, and repeated circuit simulations many times to evaluate the circuit yields.

11 Stages of AQFP gates used in the Monte Carlo simulation are shown in Fig. 1. In the simulation, the critical currents of 10 stages of AQFP gates except the first stage were scattered according to the Gaussian distribution function with the standard deviation of σ . We have prepared circuit parameters for 25,000 sets of the AQFP circuits, whose critical currents were scattered, and conducted circuit simulations to evaluate the probability of the correct operation of the circuit for different interconnect inductance $L_{\rm inp}$.

Fig. 2 shows the dependence of the correct operation probability of the 11 stages of AQFP gates on the normalized standard

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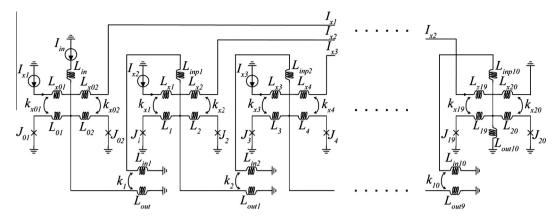


Fig. 1. 11 Stages of AQFP gates used in the Monte Carlo simulations. Critical current of the junctions of the first stage AQFP gate: $I_{c01} = I_{c02} = 50$ μA. Critical current of the junctions of 10 stages of AQFP gates: $I_{c1} = I_{c2} = \dots = I_{c20}$ (Scattered according to the Gaussian distribution function whose average value, I_{c0} is 50 μA). Coupling factors: $k_{x01} = k_{x02} = k_{x1} = k_{x2} = \dots = k_{x20} = k_1 = k_2 = \dots = k_{10} = 0.3$. Interconnect inductances between AQFP gates: $L_{inp1} = L_{inp2} = \dots = L_{inp10}$. Loop inductances of AQFP gates: $L_{01} = L_{02} = L_{01} =$

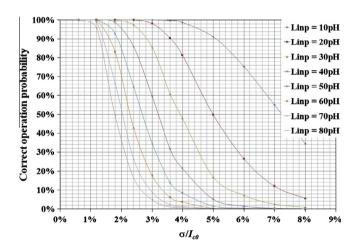


Fig. 2. The dependence of the correct operation probability of 11 stages of AQFP gates on the normalized standard deviation σ/I_{c0} of the critical current for the different values of the interconnect inductances $L_{\rm inp}$.

deviation σ/I_{c0} of the critical current for different values of the interconnect inductances $L_{\rm inp}$. It can be seen from the figure that the correct operation probability decreases with the increase of the standard deviation σ . In addition, the probability also decreases when the interconnect inductance becomes large. Therefore, an acceptable interconnect inductance $L_{\rm inp}$ exists for the given standard deviation σ , which is determined by the fabrication process.

3. Circuit yield model for large-scale AQFP integrated circuits

We will make an analytical model to estimate the circuit yields of large-scale AQFP circuits. Since the distribution of the critical current of AQFP circuits obeys the Gaussian distribution function, the model can be made based on the error function. We define the parameter $\Delta I_{\rm cRL}$, which represents the maximum allowable difference between the two critical currents of the AQFP gate for the correct operation. $\Delta I_{\rm cRL}$ can be determined by circuit simulations.

By using the ΔI_{CRL} , the correct operation probability of N stages of AQFP gates can be derived by the error function. Assuming the standard deviation of the critical current of the junctions composing AQFP circuits is σ , the standard deviation of the difference between the two critical currents of the AQFP gate is given by

Table 1 The relationship between interconnect inductance $L_{\rm inp}$ and $\Delta I_{\rm cRL}$

L _{inp} (pH)	$\Delta I_{\rm cRL} (\mu {\sf A})$
10	8.93
20	6.36
30	4.93
40	4.03
50	3.40
60	2.94
70	2.59
80	2.31

$$\sigma_{-}\Delta I_{c} = \sqrt{2}\sigma. \tag{1}$$

As stated above, the AQFP gate can operate correctly when the difference between the two critical current of the AQFP gate is within $\pm \Delta I_{\text{cRL}}$. Therefore, the correct operation probability of the AQFP gate is given by

$$P_{1} = erf \left[\frac{\Delta I_{cRL}}{\sqrt{2}(\sigma_{-}\Delta I_{c})} \right]. \tag{2}$$

by using the error function. The correct operation probability of the N stages of AQFP gates is, then, given by

$$P_N = (P_1)^N. (3)$$

The relationship between interconnect inductance $L_{\rm inp}$ and $\Delta I_{\rm cRL}$ was calculated and is listed in Table 1. The comparisons of the correct operation probabilities of the 11 stages of AQFP gates for different values of the interconnect inductances $L_{\rm inp}$ are shown in Fig. 3, where the curve represents the calculation results using Eqs. (1)–(3) and the dots are the simulation results using the Monte Carlo method. From the figure, we can find that the curve using the analytical model agrees well with the results calculated by the Monte Carlo method for the different valued of the interconnect inductance. Therefore, it can be considered that the analytical model is appropriate for calculating the circuit yields of large-scale AQFP circuits.

4. Evaluation of the circuit yield of large-scale AQFP integrated circuit

Utilizing the analysis method derived in the previous section, we will estimate the circuit yields of the large-scale AQFP circuits

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