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Memory effect in balanced Josephson comparators

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ABSTRACT

The performance of a balanced Josephson comparator is measured by its gray-zone and its maximum operation frequency. A typical effect at high clock frequencies is the correlation of output bits with their predecessors, the comparator develops a memory. This is undesirable, as it imposes an upper limit on the useful clock frequency at which the comparator can be operated.

In this work, we describe and observe experimentally the memory effect of a Josephson comparator and study its influence on the gray zone width and the maximum effective data rate.

1. Introduction

The Josephson balanced comparator is ubiquitous in analog and digital superconducting electronics. Much recent attention has been focused on the comparator *gray-zone*, a measure for the uncertainty of the comparator when the input signal is near its threshold. Thermal noise affects the instantaneous comparator threshold, making the switching process a stochastic one. This process is fairly well-understood, and an accepted model exists [1,2]. The understanding of the intrinsic timing is essential for optimization of the dynamic performance in terms of speed and sensitivity [1]. Summarised, this model assumes that the comparator switching probability is a Gaussian variable with a certain standard deviation, the so-called comparator gray-zone.

This model has proven accurate in a well-designed comparator when the frequency of the applied clock signal is sufficiently low [3,4]. In that regime, whenever the comparator switches, transient responses of previous switching events have died down sufficiently to make thermal noise (Johnson–Nyquist) the dominant influence on the instantaneous comparator threshold. Recently it has become clear that this is not the case for high frequencies [5]. In that regime, the lingering transient response of previous switching events affects the instantaneous comparator threshold, imposing a dependence of the current decision on previous decisions. We say that the comparator exhibits a *memory effect*.

In this work, we investigate this memory effect by means of simulation and measurements. We employ the ISTEC SRL standard process of AIST Japan with 2.5 kA/cm^2 critical current density [6] throughout.

2. Simulated response

2.1. Comparator circuit

The subject of our investigation is the circuit presented in 1. The decision-making pair is made up of the junctions J_2 and J_3, at the interface of which the input current is injected. A Josephson transmission line transmits the single flux quantum (SFQ) clock pulse to the top of the comparator, where the corresponding 2π phase jump of the quantum-mechanical wave function is equalised through switching of either J_2 or J_3.

If the input current is sufficiently low, then J_2 is biased closer to its critical current than J_3, supporting the switching of J_2. In this case, no output appears. If the input current is higher than the threshold, then J_3 is biased closer to its critical current than J_2, supporting J_3 switching instead. In this case, an SFQ pulse appears at the output.

2.2. Decision time

The duration of the switching events of the comparator, a random variable, determines the nature of the memory effect. The timing of our comparator from Fig. 1 was simulated, with results presented in Fig. 2. Reported are the mean comparator

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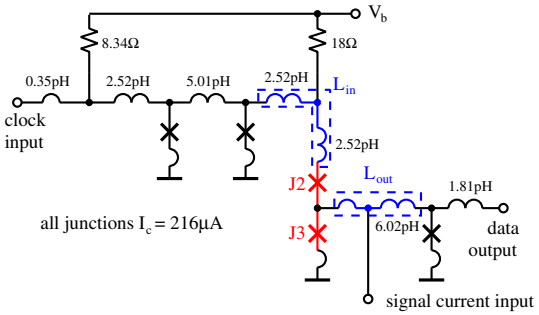

Fig. 1. Schematic diagram of the comparator circuit under investigation. The decision-making pair is made up of J_2 and J_3. All junctions are critically damped.

decision-time, τ, as well as its standard deviation (jitter), σ, both as a function of the input signal current. Note that the ordinate axis is logarithmic in both plots.

When the input signal is far away from the comparator threshold, the decision process is unambiguous, the junctions are biased in such a way that one junction has a significant advantage over the other, leading to a fast switching event. When the input signal is close to the comparator threshold, however, both junctions may be similarly biased, which means that time is required before the unambiguity resolves itself and it is decided which way the comparator will switch.

For the optimal bias of $V_b = 1.85$ mV, the peak mean switching time is $\tau_{peak} = 200$ ps. This means that at any clock frequency greater than $1/\tau_{peak} = 5$ GHz, successive clock events are likely to "collide", leading to the undesirable situation where the current switching event depends on previous switching events, the memory effect occurs.

Note that 5 GHz is significantly below the expected operating frequency of SFQ electronics implemented in the 2.5 kA/cm^2 process [7], which means that the memory effect is likely to be significant in real applications.

3. Experimental response

3.1. Baseline

To investigate the memory effect experimentally, the testbed depicted in Fig. 3 was laid out and fabricated. An on-chip high-speed clock generator enables application of a 16-bit pulse-train with adjustable frequency to the comparator. The comparator output is stored in a 16-bit shift register, from which it can be read out and processed with room temperature equipment.

To obtain a useful baseline, the comparator gray-zone was measured at low speed (with the test setup employed by Ebert et al. [8] set to a frequency of 50 kHz), as depicted in Fig. 4. The measured traces correspond to expectations. The comparator bias current is an important degree of freedom for tuning the gray-zone as well as the switching speed.

3.2. Performance indicators

The experimental low-frequency results in Fig. 4 do not show the memory effect, because the investigated frequency is too low. In this mode of operation, all decisions are fully independent. This condition is often described as a balanced comparator [4]. To obtain a performance indicator describing the memory effect, we define a quantity that measures the extent to which a comparator's decision is influenced by the previous decision, a correlation with delay 1. This quantity is defined as

$$c_1 = \frac{1}{N-1}\sum_{n=2}^{N} x[n]\cdot x[n-1], \tag{1}$$

where x is a vector of length N representing a string of consecutive comparator output bits, where $x[i] = -1$ corresponds to the absence of comparator output (binary 0) and $x[i] = 1$ corresponds to the incidence of comparator output (binary 1). We code the data in this way to ensure that each decision contributes with equal magnitude to the performance indicator.

The incidence of output bit pairs and their contribution to c_1 in a memoryless comparator can be mapped to its switching probability p. This is explained in Table 1. An intuitive understanding of c_1 results from considering the two possible values of the terms in the sum, 1 and -1, of which the former represents two consecutive switches of one and the same junction and the latter represents one switch each of J_2 and J_3. It is clear that c_1 must approach 1 if the input current is far away from the threshold, as then the same junction (J_2 or J_3) always switches.

From all four possible output pairs and their corresponding probabilities, the ideal value for c_1, the one we would expect from a memoryless comparator, is thus found in terms of p as

$$c_1 = \left(p - \frac{1}{2}\right)^2, \tag{2}$$

a parabola with its minimum, $c_1 = 0$, at $p = 0.5$, the threshold.

Especially when the input current is near the threshold, c_1 becomes a telling quantity. Near threshold, the comparator switching probability assumes 50% (cf. Fig. 4). In a memoryless comparator, the terms in the sum from (1) must take on the values 1 and -1 with equal probability, yielding $c_1 = 0$. In a comparator with

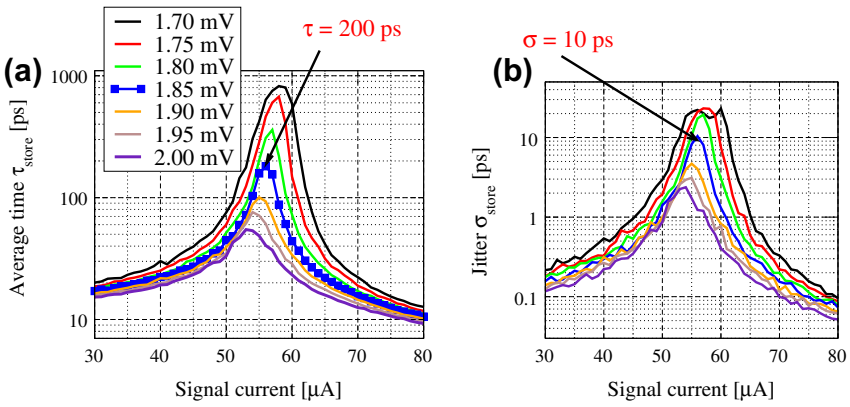

Fig. 2. Simulated decision delay (a) and timing jitter (b) of the comparator junctions.