



Superconducting gates with fluxon logics

H. Nacak, F.V. Kusmartsev *

Department of Physics, Loughborough University, Loughborough LE11 3TU, UK

ARTICLE INFO

Article history:

Available online 20 February 2010

Keywords:

Logic
Gates
Elements
Josephson
Junctions

ABSTRACT

We have developed several logic gates (OR, XOR, AND and NAND) made of superconducting Josephson junctions. The gates based of the flux cloning phenomenon and high speed of fluxons moving in Josephson junctions of different shapes. In a contrast with previous design the gates operates extremely fast since fluxons are moving with the speed close to the speed of light. We have demonstrated their operations and indicated several ways to made a more complicated logic elements which have at the same time a compact form.

© 2010 Elsevier B.V. All rights reserved.

1. Introduction

Logic gates are fundamental structures of digital circuits. Typically logic gates perform logical processes. Information of bits from the inputs are processed and a single logic output is produced. Most logic gates contain two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V). There are seven basic logic gates (AND, OR, XOR, NOT, NAND, NOR, and XNOR). The NAND and NOR gates are the universal logic gates. All other types of Boolean logic gates can be created from a suitable network of just NAND or NOR gate(s). Logic gates are mostly made of complementary metal oxide semiconductor (CMOS) transistors and diodes. Often millions or billions of logic gates are packaged in a single integrated circuit. For example the transistor count of 8-Core Intel Xeon Nehalem-EX processor is 2.3 billion. There are several logic gate design paradigms based on resistors, transistors and diodes. These are resistor–diode logic (RDL), resistor–transistor logic (RTL), diode–transistor logic (DTL), transistor–transistor logic (TTL) and complementary metal oxide semiconductor (CMOS). They have different advantages like efficiency, cost, speed, size or reliability. Logic gates have been made out of DNA, quantum mechanical effects and non-linear optical effects.

Our study is on fluxon based logic gates. We show that it is possible to produce logic gates based on fluxon dynamics using two dimensional Josephson Transmission Lines. This is a further study and application of the cloning and collision phenomena studied in [1,2]. We designed OR, AND, XOR and finally the universal logic

gate NAND. Fluxon dynamics in Josephson junctions and the potential application areas of it attracts great interest in superconducting physics [1–7]. The electrodynamics of a Josephson Transmission Line is described by 2D sine-Gordon equation. The normalized equation is written as

$$\varphi_{tt} - \nabla^2 \varphi + \alpha \varphi_t + \sin(\varphi) = 0 \quad (1)$$

Here $\alpha = 1/\sqrt{\beta_c}$ is the dimensionless damping parameter (β_c is McCumber–Stewart parameter). The spatial coordinates are normalized to the Josephson penetration depth λ_c . Time is normalized to the inverse of the plasma frequency w_p^{-1} , velocity u is normalized to the Swihart velocity $\bar{c}(\bar{c} = \lambda_j W_p)$ and the energy is normalized to $j_c \lambda_j^2 \Phi_0 / 2\pi$ ($\Phi_0 = h/2e$ is the magnetic flux quantum). We used the orthogonal coordinates and Neumann boundary conditions $\mathbf{n} \cdot \nabla \varphi|_{\partial\Omega} = 0$. For calculation we used the Comsol Multiphysics finite element program package.

An important solution of Eq. (1) is the sine-Gordon soliton which describes the dynamics of the superconducting phase difference

$$\varphi(x, y, t) = 4 \arctan \exp \left(\frac{x - x_0 - ut}{\sqrt{1 - u^2}} \right) \quad (2)$$

and the energy of the soliton in two dimensional junction with width W is

$$E = \int_{-\infty}^{\infty} dx \int_0^{W(x)} dy \left[\frac{\varphi_t^2}{2} + \frac{\nabla \varphi^2}{2} + 1 - \cos \varphi \right] \quad (3)$$

We use fluxons, antifluxons, synchronized fluxons and fluxons–antifluxons as information bits to represent the voltage levels in the conventional logic gates. The binary conditions of the inputs

* Corresponding author.

E-mail address: F.Kusmartsev@lboro.ac.uk (F.V. Kusmartsev).

are: If no fluxon exists on input or on output this corresponds to low voltage (0) and existing of a fluxon corresponds to high voltage (1).

2. OR gate

In Boolean algebra the OR gate gives an output 1 if either or both of the inputs are 1. Table 1 (also known as the truth table) shows the output states for possible combination of input states. For representing the OR gate we have used Y shaped Josephson

Table 1
Truth table for OR gate. A and B are inputs and Q is output. The OR gate gives an output 1 if either or both of the inputs are 1.

A	B	Q
1	0	1
0	1	1
0	0	0
1	1	1

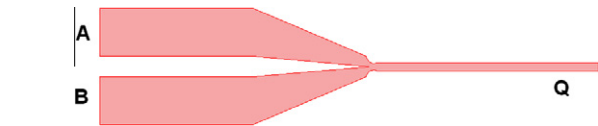


Fig. 1. OR gate represented by Y junction. A and B are inputs and Q is output.

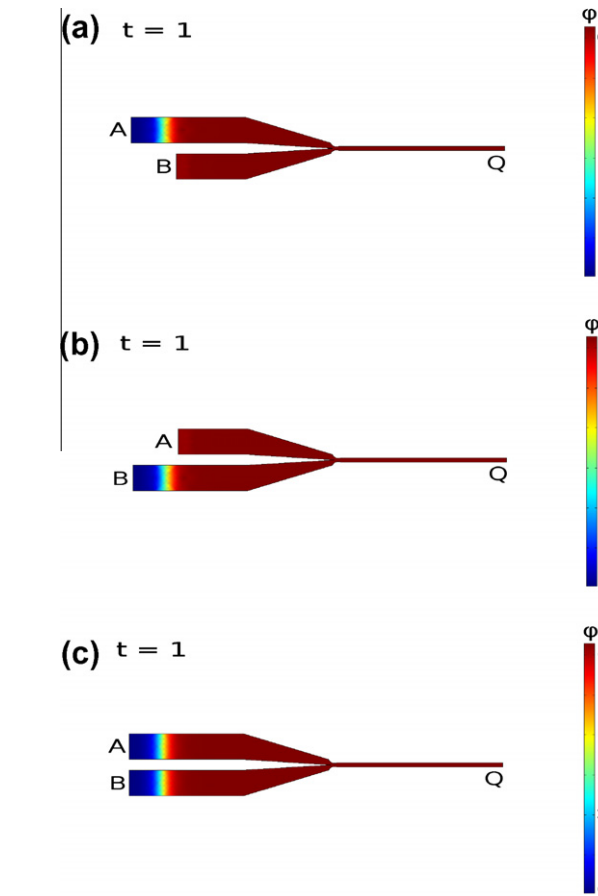


Fig. 2. OR gate with a single fluxon starting to move from input A (a), B (b) and both A and B (c).

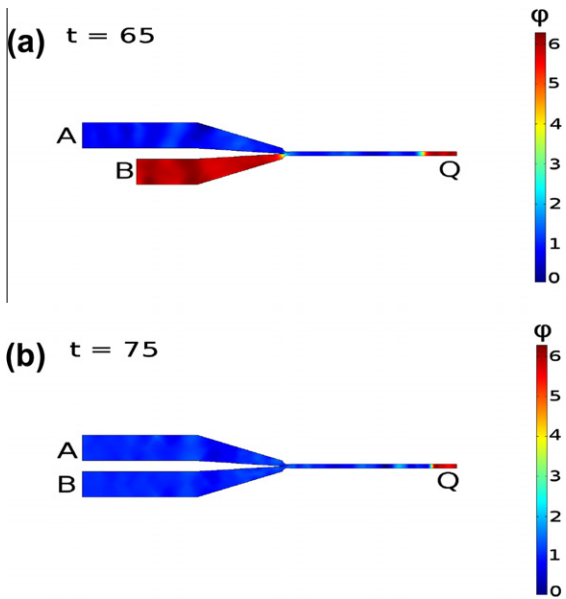


Fig. 3. OR gate with a single fluxon (a) and a united single fluxon (b) moving to the output Q.

Transmission Line shown in Fig. 1. Here A and B indicates the input and Q indicates the output. The numbers 1 and 0 in the table show whether there is a fluxon or not.

In Fig. 2, a fluxon with velocity $u = 0.3$, $\alpha = 0.001$ and $x_0 = -25$ is propagating in the JTL inserted from input A (Fig. 2a) or input B (Fig. 2b) or both inputs (Fig. 2c) and reaches the output Q (Fig. 3a and b). It is obvious that if there is no fluxon on the inputs there will also none on the output. So the conditions in the first three rows in Table 1 are provided.

To fulfill the condition in the last row in Table 1 two fluxons are inserted from inputs A and B at the same time (Fig. 2c) and each with the same energy E. The fluxons are merging where the arms of the Y junction meets and from this point on a united single fluxon with energy $2E$ (Fig. 3b) is moving to the output Q.

Summation of the energies is a key feature. Later on we will use this property to construct the AND gate, NAND gate and complex Josephson networks.

3. XOR gate

In XOR gate when both inputs are the same then the output is 0 otherwise 1. The notation B_{af} in Table 2 denotes that only antifluxon-

Table 2
Truth table for XOR gate. The notation B_{af} denotes that only antifluxons are inserted from input B and the minus sign denotes the opposite polarization of the antifluxon.

A	B_{af}	Q
1	0	1
0	-1	-1
0	0	0
1	-1	0

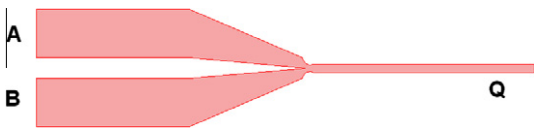


Fig. 4. XOR gate also represented by Y junction.

Download English Version:

<https://daneshyari.com/en/article/1818813>

Download Persian Version:

<https://daneshyari.com/article/1818813>

[Daneshyari.com](https://daneshyari.com)