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Resistor-less charge sensitive amplifier for semiconductor detectors

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ABSTRACT

A new concept of a Charge Sensitive Amplifier without a high-value resistor in the feedback loop is presented. Basic spectroscopic parameters of the amplifier coupled to a coaxial High Purity Germanium detector (HPGe) are discussed. The amplifier signal input is realized with an n-channel J-FET transistor. The feedback capacitor is discharged continuously by the second, forward biased n-channel J-FET, driven by an RC low–pass filter. Both the analog—with a standard spectroscopy amplifier and a multi-channel analyzer—and the digital—by applying a Flash Analog to Digital Converter—signal readouts were tested. The achieved resolution in the analog and the digital readouts was 0.17% and 0.21%, respectively, at the Full Width at Half Maximum of the registered ^{60}Co 1332.5 keV gamma line.

1. ntroduction

In ultra-low background experiments searching for rare nuclear processes at low energies the tolerable contamination of the detectors components with radioactive isotopes are extremely low. Projects such as GERDA [1] and MAJORANA [2] employ HPGe detectors, both as the source and the target for observation of neutrino-less double beta decay of ^{76}Ge. The signal readout is typically realized through a charge sensitive amplifier located very close to the HPGe crystals. Therefore while designing the Very Front End (VFE) electronics one must take into account the background budget of the experiment [3,4].

One of the main identified internal sources of the ionizing radiation in the classical architecture of the Charge Sensitive Amplifier (CSA) is a high resistivity (typically the order of GΩ) feedback loop resistor. Materials used for fabrication of the commercially available resistors (Surface Mount Devices, SMDs) are hardly radio-pure. Several options for custom-made feedback resistors were considered: amorphous germanium [5], titanium nitride (TiN) thin film resistors or tungsten (W) on a quartz substrate [6]. Unfortunately they all showed stability problems that would need to be solved for a long-term (time scale of years) operation of the experiments. Several approaches to the resistor-less CSA architecture were recently proposed, like double-gate double-feedback J-FET charge-sensitive preamplifier [7] or CSA with a pulsed mode reset. The former approach is intended for dedicated semiconductor structures, like double-gate J-FETs [8] or J-FETs with an exposed substrate. The latter design requires an additional reset circuitry (a comparator, pulse generator, analog switches) and exhibits limitations with respect to the dynamic range of some Analog to Digital Converters (ADCs).

The resistor-less CSA, described in this paper, exhibits very good spectroscopic parameters (energy resolution), low number of components, and a simple design and construction. All these features all highly desirable for ultra-low background applications.

2. Design of the resistor-less charge sensitive amplifier

The circuit of the new resistor-less CSA is shown in Fig. 1. Two feedback loops are used to separate the fast (high frequency) and the slow (down to DC) components of the feedback signal. The slow feedback loop is placed in lieu of the classical single high-value resistor. The high frequency response is ensured by the feedback capacitor C_F, responsible for integrating the current pulses from the detector coupled to the input. Operating point of the amplifier is governed by the detector input leakage current and the slow feedback loop, composed of the low-pass RC network ($R_1 \parallel R_2 \cdot C_S$ defining the C_F discharge time constant), R_2 and T_2. DC output offset fine adjustment is possible using R_1R_2 voltage divider. In the steady state, the detector leakage current flows into the T_2 gate and through R_2 (small comparable to the T_2's gate resistance r_G) to the negative power supply V_{SS}, also providing a path to discharge the feedback capacitor C_F.

Temperature drifts and leakage current fluctuations are controlled by the negative feedback of the CSA output voltage, realized with T_2. Transfer characteristic of the CSA is given by the charge amplification factor $k_q = v_{out,max}/Q_i$, where $v_{out,max}$ is the maximum CSA voltage response for a given input charge Q_i. Following the analysis presented e.g. in [7], the general transfer

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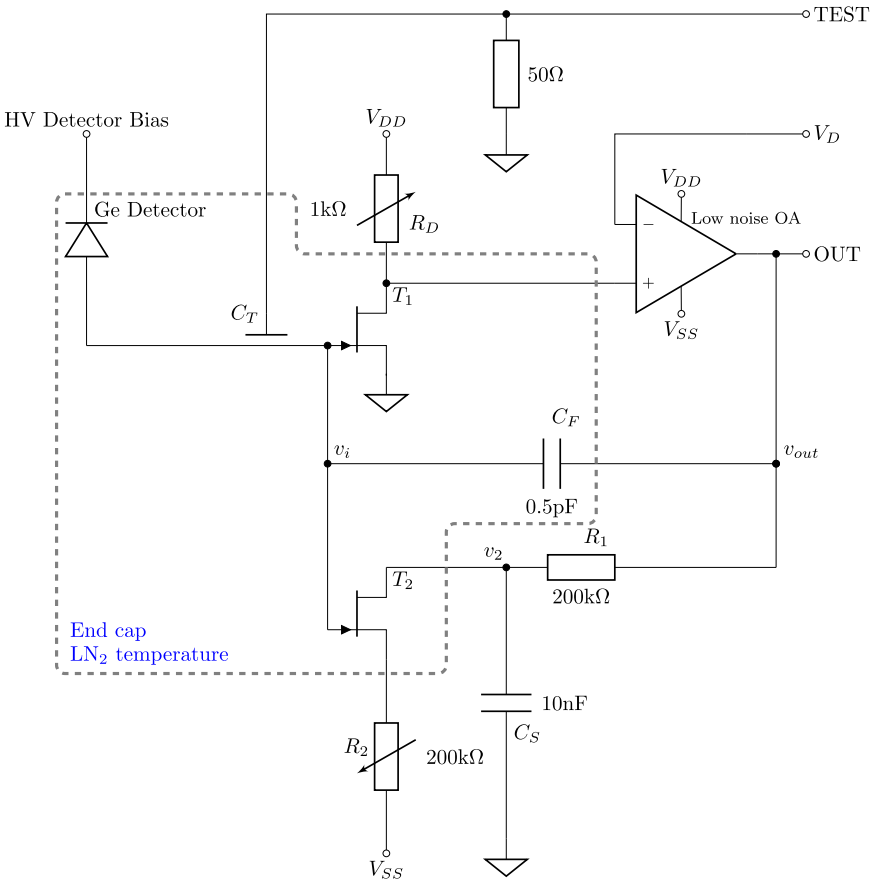

Fig. 1. The simplified schematics of the developed resistor-less Charge Sensitive Amplifier. The couple of transistors is placed very close to the detector. C_F closes the high frequency feedback loop, while T_2, C_S and $R_1 \parallel R_2$ form the low frequency loop (to discharge C_F). V_D sets the drain–source voltage of T_1, while R_D is used to control T_1's drain current.

function is given by the set of equations:

$$0 = i_{det} - v_i\left(sC_D + s2{\cdot}C_G + \frac{1}{r_G}\right) - v_2\frac{1}{r_G} - v_{out}sC_F \tag{1a}$$

$$v_2 = v_{out}\frac{1}{1+s\tau} \tag{1b}$$

$$v_{out} = -Kv_i \tag{1c}$$

$$\tau = R_1 \parallel R_2{\cdot}C_S \tag{1d}$$

where K is the open loop gain of the operational amplifier, including the inverting input J-FET stage. The open loop gain K is assumed to be frequency-independent ($K(s) \triangleq K$), and large. i_{det} is the detector current, approximated by the delta function $i_{det} = Q_i\delta(t)$. C_D is the detector capacitance, C_G is the input gate capacitance of T_1 and T_2, r_G is the gate resistance of the forward biased T_2, and v_2 is the voltage at T_2 drain. The solution of Eq. (1a) reads:

$$\frac{v_{out}}{i_{det}} = \frac{r_G(1+s\tau)}{1 + sr_GC_F + s^2\tau\, r_GC_F - \dfrac{r_G(1+s\tau)}{K}\left(sC_D + s2{\cdot}C_G + \dfrac{1}{r_G}\right)} \tag{2}$$

For large K it simplifies to:

$$\frac{v_{out}}{i_{det}} = r_G\frac{1+s\tau}{1+s\tau_G + s^2\tau\tau_G} \tag{3}$$

where $\tau_G = r_GC_F$, with approximate poles $s = -\frac{\tau_G+\tau}{\tau\tau_G}$ and $s = -\frac{1}{\tau_G}$, i.e. the fast and the slow components of the output signal. Also, a detailed SPICE[1] model of the described amplifier was constructed, reproducing well the observed pulse response of the circuit with a 30 pF dummy detector. As an example, the amplifier output to a 1 V test step pulse (10 ns rise time) is shown in Fig. 2. The calculated (simulated) signal rise time is less than 125 ns, time constant of the CSA is set to 44 μs.

3. Test setup

An electronic chain, used for an ionization signal readout, usually consists of a charge sensitive (pre)amplifier, a linear amplifier conditioning the signal and driving the transmission line (referred to as the Frond End, FE), and a signal digitizer (a Flash Analog to Digital Converter, FADC). In an analog readout system, the signal representing the energy deposit in the detector, is quantized by a multi-channel analyzer, after passing a shaping amplifier.

A DSG 1810 p-type HPGe detector (coaxial crystal in a vacuum cryostat, 10% relative efficiency, FWHM = 1.8 keV with a standard CSA according to the technical specification) was used to test the new amplifier. The input J-FET transistors and the feedback

[1] Simulation Program with Integrated Circuit Emphasis, SPICE. The model was implemented in the TINA-TI V9 program (Texas Instruments).