Nuclear Instruments and Methods in Physics Research A 780 (2015) 33–39

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

A data acquisition system for two-dimensional position sensitive micropattern gas detectors with delay-line readout

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ARTICLE INFO

Article history:
Received 16 September 2014
Received in revised form
13 January 2015
Accepted 14 January 2015
Available online 23 January 2015

Keywords:
Delay-line readout
Image acquisition system
Time-to-digital converter
FPGA
Micropattern gas detectors

ABSTRACT

We present a data acquisition (DAQ) system for two-dimensional position sensitive micropattern gas detectors using the delay-line method for readout. The DAQ system consists of a field programmable gate array (FPGA) as the main data processor and our time-to-digital (TDC) mezzanine card for making time measurements. We developed the TDC mezzanine card around the Acam TDC-GPX ASIC and it features four independent stop channels referenced to a common start, a typical timing resolution of ~81 ps, and a 17-bit measurement range, and is compliant with the VITA 57.1 standard. For our DAQ system, we have chosen the Xilinx SP601 development kit which features a single Spartan 6 FPGA, 128 MB of DDR2 memory, and a serial USB interface for communication. Output images consist of 1024×1024 square pixels, where each pixel has a 32-bit depth and corresponds to a time difference of 162 ps relative to its neighbours. When configured for a 250 ns acquisition window, the DAQ can resolve periodic event rates up to 1.8×10^6 Hz without any loses and will report a maximum event rate of 6.11×10^5 Hz for events whose arrival times follow Poisson statistics. The integral and differential non-linearities have also been measured and are better than 0.1% and 1.5%, respectively. Unlike commercial units, our DAQ system implements the delay-line image reconstruction algorithm entirely in hardware and is particularly attractive for its modularity, low cost, ease of integration, excellent linearity, and high throughput rate.

1. Introduction

Typically, the most suitable readout technique for position sensitive micropattern gas detectors is the direct pixel readout. In this approach, the charge collecting anode is segmented into pixel structures which are individually connected to their own pulse processing electronics. To obtain good spatial resolution, the pixel size should match electron diffusion within the gas and a large effective area requires a large number of pixels. Detectors based on the Gas Electron Multiplier (GEM) or the THick Gas Electron Multiplier (THGEM) are particularly well-suited for the direct readout technique due to having separate amplification and readout regions. This unique feature allows optimization of the readout structure according to the requirements of the imaging application. Using a highly segmented direct pixel readout, [1] showed that the primary ionization clusters within a triple-GEM detector can be resolved with ~50 μm spatial resolution [1]. However, due to the large number of electronic channels required, the direct pixel readout is limited by cost to small effective areas. Consequently, alternative readout techniques are always being considered.

Interpolating readout techniques, such as resistive charge division or delay-line timing, can significantly reduce the number of electronic channels by measuring a position dependent parameter, such as signal amplitude or elapsed time. Delay-line timing is a commonly used interpolating readout technique whereby the interaction position of events within a detector is encoded in the time difference between a pair of signals. Using the delay-line approach, a two-dimensional readout can be constructed with only four electronic channels and an external trigger. Electromagnetic delay-lines are often categorized as distributed parameter or lumped parameter delay-lines. Whereas distributed parameter delay-lines are based on the transmission line properties of coaxial cables or microstrips, lumped parameter delay-lines resemble symmetrical networks of discrete inductors and capacitors. Using either approach, delays in the range of a few hundred picoseconds to hundreds of microseconds are possible. In practice, lumped parameter delay-lines are preferred since they occupy smaller volumes and are less attenuating than distributed parameter delay-lines.

In addition to the small number of electronic channels, the delay-line readout is preferred for its simple construction, immunity to

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http://dx.doi.org/10.1016/j.nima.2015.01.053
0168-9002/

signal amplitude variations, and excellent position resolution. Due to an inherent center-of-charge averaging, the position resolution of detectors employing a delay-line readout is often better than the electrode pitch spacing. By comparison, direct pixel readouts require center-of-charge averaging to be implemented in post-processing, thus introducing an additional level of complexity. However, unlike the direct pixel readout which can resolve multiple events in coincidence, a delay-line readout is limited to single events within the acquisition window. Consequently, the event rate capabilities of the delay-line readout are directly limited by the total delay-line length and the electronic dead time required to process an event. Nevertheless, it has been demonstrated that position sensitive GEM detectors, coupled to fast delay-lines, can handle event rates in excess of 10^5 Hz per mm^2 [2–5]. Furthermore, stereo angle readouts employing delay-line timing have demonstrated the possibility of resolving multiple events in a single acquisition window [2].

Traditionally, delay-line signals are analyzed using a pulse processing chain which consists of fast current pre-amplifiers, filtering amplifiers, constant fraction discriminators (CFD), and time-to-amplitude converters (TAC). While the first part of the chain prepares the signals for timing pick-off, the TAC produces an analog voltage pulse with an amplitude that is proportional to the time difference between delay-line signals. The TAC signal is digitized by an analog-to-digital converter (ADC) and the digital value is used to address a memory location which corresponds to the reconstructed event position. However, TAC and ADC based acquisition systems exhibit poor event rate capabilities due to the long analog-to-digital conversion time [6,7]. Furthermore, the time resolution is constrained by the full scale range and the number of digitization bits available on the ADC. Consequently, a tradeoff exists between the maximum measurable time difference and resolution.

Time-to-digital converters (TDCs) directly digitize the time intervals by using a high frequency clock and an interpolator circuit [8]. As such, TDCs exhibit fast conversion times and resolutions which are independent of the full scale range. Commercially available TDCs are capable of periodic event rates in bursts of 100 MHz and timing resolutions down to a few picoseconds [9]. However, there are currently no available TDCs which can implement the delay-line reconstruction algorithm in real time and on an event-by-event basis. Instead, the user must transfer the time measurements for each event to a computer and perform the reconstruction. Since a large overhead is transmitted with each time measurement, the event rate capabilities of such a system are at least one order of magnitude slower than a hardware implementation. By connecting the TDC directly to a hardware processor, such as a field programmable gate array (FPGA), the delay-line reconstruction algorithm can be performed in parallel with the acquisition and therefore capable of higher event rates. By using a commercially available TDC ASIC and FPGA carrier board, we demonstrate that it is possible to build a delay-line acquisition system which can process up to a few million events per second.

In this work, we present a digital data acquisition (DAQ) system for position sensitive micropattern gas detectors with delay-line readout. Consisting of a commercial FPGA carrier board and our TDC mezzanine card, the DAQ features four independent stop channels referenced to one global start channel, a typical timing resolution of 162 ps, and a 17-bit measurement range. By using a modular design approach, we managed to significantly reduce prototyping times and cost without sacrificing features often found in purpose built systems. Moreover, we have demonstrated that the DAQ can process periodic event rates up to 1.8×10^6 Hz while the integral and differential non-linearities are better than 0.1% and 1.5%, respectively. In this paper, we discuss the hardware architecture, firmware architecture, and system performance of our DAQ system. The imaging capabilities of the DAQ have been successfully verified using our general purpose THGEM imaging detector [10] and will also be presented.

2. Hardware architecture

Owing to the growing popularity of FPGAs in embedded systems, various industry standards have been established which allow a single FPGA design to be reused for a wide range of applications. These standards enable modular system design by separating the FPGA from the input/outputs with a carrier to mezzanine card approach. The most recent standard – VITA 57.1 [11] – is supported by major FPGA vendors Xilinx and Altera. In the VITA 57.1 standard, mezzanine cards are mated with FPGA carrier boards via an FPGA Mezzanine Card (FMC) connector. As long as sufficient I/O pins are mapped to the FMC connector, the FPGA carrier board can be configured to support the mezzanine card.

To minimize prototyping time and cost, our DAQ system is implemented using a modular hardware architecture which is compliant with the VITA 57.1 standard. The DAQ consists of three main components: a TDC mezzanine card which receives the delay-line signals from the CFD and makes time measurements, a commercial FPGA carrier board which generates the X and Y coordinates and performs hardware histogramming of the incoming events, and a PC which displays the images and controls the system.

Our TDC mezzanine card, shown in Fig. 1a, measures 69 mm $\times$ 76.5 mm and integrates with compatible FPGA carrier boards through an FMC low pin count (LPC) connector. The hardware architecture of the TDC mezzanine card, shown in Fig. 1c, centers around the TDC-GPX [9] ASIC which features 9 LVTTL inputs (1 start, 8 stops), a temperature stable time resolution of 64–113 ps, 5.5 ns pulse pair resolution, a 17-bit measurement range, and up to 40 MHz continuous rate per chip. Of the 9 LVTTL inputs, our TDC mezzanine card uses only the start and 4 stop inputs for processing the delay-line signals.

The high temporal resolution of the TDC-GPX is achieved through internal gate propagation delays which are susceptible to changes in core voltage and temperature unless stabilized. To overcome this, the TDC-GPX regulates its core voltage against temperature fluctuations by controlling an external feedback signal connected to the power supply. At the maximum operating temperature the maximum core voltage is reached while the minimum core voltage is reached at the lowest temperature. The feedback control signal is generated by an internal phase locked loop (PLL) circuitry. An external 40 MHz clock provides the base PLL frequency and resolution calibration. Using this scheme, the TDC-GPX achieves temperature stable timing resolution between -40 °C and $+125$ °C.

To interface the TDC-GPX with common timing pick-off electronics, NIM-to-LVTTL circuits were included for each of the five inputs on the TDC mezzanine card. The NIM-to-LVTTL circuits interface the two logic standards by comparing the fast NIM signals against an appropriate threshold level (-500 mV). To compare the fast NIM signals and threshold levels, the Linear Technology LT1715 comparator was selected for its small output timing jitter and fast toggling frequency. The LT1715 has a maximum toggling frequency of 150 MHz and an output timing jitter of 15 ps RMS. Although the LT1715 offers dual comparators in a single package, this feature was not used due to significant cross-talk between neighbouring channels exhibited at high switching frequencies.

The complete DAQ system, shown in Fig. 1b, is assembled by mating our TDC mezzanine card with a Xilinx SP601 development kit. The Xilinx SP601 is a commercial FPGA carrier board which