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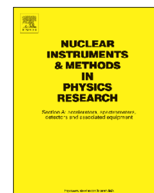

Advantages of a vertical integration process in the design of DNW MAPS ☆

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A B S T R A C T

This work discusses the main features of a CMOS Deep N-well (DNW) monolithic active pixel sensor (MAPS) fabricated in a vertically integrated technology, where two 130 nm CMOS homogeneous tiers are processed to obtain a 3D integrated circuit (3D-IC). The 3D CMOS MAPS, which was designed in view of vertexing applications to experiments at high luminosity colliders, features a 20 μm pitch for a point resolution of about 5 μm and data sparsification capabilities for high data rate systems. Results from the characterization of different test structures, including single pixels, 3×3 and 8×8 matrices, are presented. In particular, measurements have been performed with an infrared laser source to evaluate the charge collection properties of the proposed vertically integrated sensors.

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1. Introduction

The need for charged particle trackers with the capability for precise momentum measurement at the future high luminosity colliders (like the B-factories or the International Linear Collider [1,2]) has prompted several research groups in the particle physics community to explore solutions involving the use of the so-called monolithic active pixel sensors (MAPS) in CMOS technology. While the spatial resolution they can achieve in imaging applications (the field where they first emerged [3]) is much higher than required of particle trackers, on the other hand they can provide an attractive solution to the design of multilayer thin detectors. In a monolithic sensor, the readout electronics is fabricated in the same substrate as the detector. Also, a large part of the mostly undepleted substrate can be removed with no significant signal loss [4], leaving only a thin sensitive layer, a few tens of micrometer thick, where charge is collected by diffusion and/or drift. In recent years, the feasibility of large, highly granular arrays of deep N-well (DNW) CMOS monolithic active pixel sensors [5] with fast readout architecture has been demonstrated [6]. DNW MAPS takes advantage of the properties of triple well structures to implement a collecting electrode with relatively large area (as compared to standard three transistor MAPS) and includes PMOS devices (avoided in standard MAPS in order not to substantially degrade the collection efficiency) in the design of high gain amplifiers and fully CMOS digital blocks at the elementary cell level. Other attempts to incorporate PMOS devices in the front-end design of MAPS sensors have been involving different technological solutions, as in the case of monolithic sensors in silicon-on-insulator [7] and quadruple well [8] CMOS processes. While being a promising approach, DNW MAPS in planar CMOS technology may still suffer from a few drawbacks (some of them actually not specific to DNW MAPS):

- the higher degree of functional complexity of the pixel level circuits made possible by the DNW MAPS approach and by the use of PMOS transistors comes at the expense of a larger area and pitch and, consequently, of a larger point resolution;
- in general, in mixed-signal circuits, analog performance may be deteriorated by coupling with the digital section through the common substrate and/or due to capacitive coupling among signal and power lines; this may be even worse in the case of monolithic sensors, where also the collecting electrode shares the same substrate with the digital circuits inside the individual pixel;
- the presence of PMOSFETs in the pixel cell, as small the taken fraction of pixel area might be, may degrade the collection efficiency of the device; inside the elementary cell, the collection efficiency may be fairly non-uniform, depending on the position of the PMOS transistors and of their N-well.

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While not being the only option, vertical integration technologies (also known as 3D integration technologies) may overcome the above-mentioned issues by hosting the analog and the digital sections in different tiers, at some cost in terms of a higher fabrication complexity [9]. Vertical integration processes for the development of high energy physics instrumentation have been explored in the framework of the 3D-IC Consortium [10]. The 3D-Integrated Circuit (3D-IC) technology consists of stacking two or more layers and connecting them vertically to achieve a single, monolithic device. The main expected advantage of using an homogeneous 3D integrated technology [11] in DNW MAPS sensors, besides the potential for increased functionality, is the reduction of the competitive PMOS N-well area, which may improve charge collection properties and in-pixel charge collection uniformity. Moreover, placing the digital blocks on a different layer from the sensor and the analog front-end improves the electrical isolation between the digital section and the most sensitive parts of the cell. In a two layer 3D process, one tier is thinned down to around 10 μm and then aligned and bonded to a second, thicker layer that also provides mechanical support. The use of a wafer thinning technique, while not affecting the charge collection properties in a DNW MAPS device, reduces the amount of material of the 3D chip. This work discusses some results from the characterization of a fine pitch DNW MAPS sensor, called SDR1 (Sparsified Digital Readout) and fabricated in a 3D 130 nm CMOS technology. The paper will be particularly focused on emphasizing the most important performance improvement related to the use of a vertical integration technology in the design of a DNW monolithic sensor.

2. Functional complexity

The SDR1 sensor was designed in a dual-tier 130 nm CMOS vertical integration process with through silicon vias (TSVs) provided by Tezzaron Semiconductor and Globalfoundries [12]. The test structures include single pixel elements, 3×3 arrays, small 8×8 and 16×16 matrices and a large, almost experiment-scale, 240×256 matrix, all with a 20 μm pitch. The front-end channel, integrated in each individual cell and including an analog and a digital section, is shown in Fig. 1. In each pixel, the bottom layer includes the deep N-well sensor, whose signal is processed by a charge sensitive amplifier (CSA) placed in the same tier. The CSA is followed by a threshold discriminator, with an NMOS differential input pair, integrated in the bottom tier and a mirrored PMOS load, integrated in the top tier to minimize the amount of PMOS transistors around the collecting electrode. Actually, a few PMOS devices, namely those used in the charge sensitive amplifier, were kept in the bottom layer. This was done, first of all, to avoid that some or all of those PMOS sat in the same layer with the logic section of the pixel, with the risk that digital signals coupled with their terminals and with some critical nodes in the CSA. Another motivation lies in the fact that having the NMOS of the CSA in one layer and the PMOS in the other one would make the design rather complicated, with a considerable amount of wiring going from one layer to the other, and the final circuit less reliable. The performance of the analog section is summarized in a work by the same authors of the present paper [13]. The top tier also includes a number of digital blocks taking care of double-hit detection with the relevant time stamping, data sparsification and pixel masking. Readout is based on a token passing architecture [14]. The operation of the detector (described in a published paper [15], together with the meaning of the signals appearing in Fig. 1) has been tailored on the beam structure of the International Linear Collider, which will feature 2820 bunches per train, each train lasting slightly less than 1 ms, with an inter-bunch period of 330 ns and a repetition rate of 5 Hz (corresponding to a duty cycle of 0.5%) [16]. Data sent-off by the pixels (X and Y coordinates and time stamps) during the readout phase are serialized by means of a multiplexer located in the top tier, at the periphery of the MAPS matrix (not shown in the figure). The SDR1 MAPS sensor represents the evolution of another monolithic detector, the SDR0 chip, previously designed and fabricated in a planar, 130 nm CMOS technology [17]. The elementary cell in the SDR0 DNW MAPS sensor featured a 25 μm pitch and was capable of storing a single hit, with the relevant time stamp, in each single bunch train period. As indicated in Fig. 1, the digital circuits integrated in the SDR0 pixel correspond, just with minimal changes, to about half of the digital front-end section of the SDR1 DNW MAPS. The latter is actually capable of storing two hits and the relevant time stamps during a bunch train, while featuring a smaller pitch. Therefore, the use of a vertical integration technology makes it possible to reach a far better compromise between the amount of integrated functions and the detector point resolution. Note that, in the specific application foreseen for the SDR1 chip, the detection efficiency is also improved with respect to the SDR0 sensor, because not only the pixel occupancy is decreased due to the smaller pixel pitch, but also the number of storable hits is doubled and the probability of hit loss due to multiple hits in the same bunch train is accordingly reduced.

3. Digital signal coupling

In mixed-signal chips, as is the case for the front-end electronics for DNW MAPS, one very obvious way to take advantage of 3D integration is by separating the analog from the digital section. As compared to planar microelectronic circuits, where analog stages have to share the same substrate with logic blocks, vertical integration may improve the immunity of the analog circuitry to the noise induced by digital activity. In MAPS sensors, also the collecting electrode is located in the same substrate as the readout electronics, which makes the requirements for isolation between the analog and the digital sections (and between the sensing electrode and the digital circuits) even tighter. In the case of the SDR1 monolithic sensor, satisfactory results have been achieved by placing all the digital blocks (hit and time stamp registers, data sparsification circuits) in the top layer of the 3D structure, while the radiation sensitive volume and the charge preamplifier (as shown in Fig. 1) are located in the bottom layer, that is, in a different substrate. As a representative example of the behaviour of the device in terms of digital signal coupling, Fig. 2(a) shows the signal at the preamplifier output in one cell of an 8×8 DNW MAPS matrix when the time stamp clock signal is present (thicker line) and when it is not (thinner line). Fig. 2(b) shows the digital signal fed to the circuit as the time stamp clock signal during the test. This is actually the only switching digital signal provided to the chip in the real operation during the detection phase, when the cell is enabled to detect a hit [15]. The time stamp clock is not sent directly to each of the matrix cells. It is actually fed to a 5 bit grey counter at the chip periphery, which in turn provides the 5 bits for the time stamp (`Time stamp in` signal in Fig. 1) to the entire matrix. The 5 bits are then frozen in the individual cell as soon as it detects an event. The frequency used in the real experiment for the time stamp clock is slightly larger than 30 kHz, since the 5 bit time stamp registers have to span the entire bunch train period, lasting, as mentioned above, about 1 ms. Therefore, given the relatively small frequency value, distribution of the time stamp can be performed by using a small number of repeaters, namely one per row, each featuring about twice the minimum size. The same strategy (one repeater per row) was used for all the arrays in the test structures (with the exception of the 3×3 matrices, which, by design, have no working digital section). The CMOS (0–1.2 V) clock signal used in the test has a 100 kHz frequency, about three times larger than in the real application, and a slew-rate of about 12 V/μs on the leading and trailing edges. In Fig. 2(a), while some glitches, correlating with the rising edge of the time stamp clock signal, can be observed in the preamplifier response when the digital signal is present, their

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