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A new digital pulse power supply in heavy ion research facility in Lanzhou

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ABSTRACT

To meet the increasing requirements of the Heavy Ion Research Facility in Lanzhou-Cooler Storage Ring (HIRFL-CSR), a new digital pulse power supply, which employs multi-level converter, was designed. This power supply was applied with a multi H-bridge converters series-parallel connection topology. A new control model named digital power supply regulator system (DPSRS) was proposed, and a pulse power supply prototype based on DPSRS has been built and tested. The experimental results indicate that tracking error and ripple current meet the requirements of this design. The achievement of prototype provides a perfect model for HIRFL-CSR power supply system.

1. Introduction

Heavy Ion Research Facility in Lanzhou-Cooler Storage Ring (HIRFL-CSR) is the first dedicated heavy ion synchrotron facility in China, which consists of a main ring, an experimental ring and a radioactive beam line [1]. Such heavy ion synchrotron complex has been used for many applications, for example, heavy ion nuclear physics research, cancer therapy and material science.

As a synchrotron [2], CSR needs variable magnetic field; therefore, power supplies work in pulse mode to provide variable excitation current for magnets so as to generate the magnetic fields the accelerator needing. The operation cycle of a CSR power supply is shown in Fig. 1. There are more than 400 power supplies in CSR. Their power are usually less than 100 kW [3], so switching technology and Pulse Width Modulation (PWM) are most appropriate for them. All power supplies in CSR were controlled in analog mode in the past.

With the development of modern accelerator technology, the smaller tracking error, faster operation cycle, and more intelligent man-machine interface are becoming the most important characteristics of accelerator power supply field. The analog power supply cannot meet the above requirements, so a new kind of power supply – the digital power supply has appeared in recent years, and various digital control power supplies are applied in accelerator power supply system rapidly [4]. Due to the great advantages and excellent performance, the digital power supply has replaced the analog one step by step. It is necessary to develop a new digital pulse power supply for heavy ion accelerator. This paper focuses on a digital pulse power supply design of CSR based on FPGA.

2. Prototype design

All power supplies in CSR must be operated synchronously [5]. Terminal timing method is adopted in CSR system: a pulse power supply receives two synchronization events in each cycle. The power supply will prepare the data of next current waveform once the first event comes. Then the power supply will put out current as soon as it receives the trigger synchronization event. In order to cut down the amount of data from the remote computer to the control card, the reference waveform is usually with a large time step (2048us). The raw waveform must be changed into a waveform with a small time step (8 or 16 μs) by interpolating before outputting; therefore, two stringent functions should be achieved for digital pulse power supply: one is doing complex mathematical calculations and the other is matching synchronization events accurately.

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2.1. Design parameter

A prototype of digital pulse power supply, which is used to feed a dipole magnet, was designed at first. The detailed specification can be found in Table 1 [6]: the short ramp time and small tracking error are worthful. Current ramp up speed is required to be as fast as 1150 A/s with an overall precision class of 100 ppm. The output voltage depends on the current waveform and the magnet inductance. As formula (1), the peak voltage is picked up as 185 V in order to reserve margin. A 2000 A/10 V DCCT is used to measure the output current. A sufficient input dc voltage and a converters topology of series-parallel connection are proposed to ensure that the current can rise from bottom to peak 1150 A in one second. Closed loop control is applied in the system to meet the current rising speed and tracking error requirements by regulating the duty cycle of DC–DC converter.

$$v_0 = IR + L\frac{dI}{dt} \tag{1}$$

Main ring dipole power supply for HIRFL-CSR is a typical pulse power supply, which employed analog solution. Its performance influences the beam quality primarily, so the main ring dipole power supply has the most stringent requirements in CSR power supply system. In spite of the digital power supply prototype's power is not as high as main ring dipole power supply, it would have more stringent performance requirements, such as higher current ramp up speed, smaller tracking error and relative ripple current.

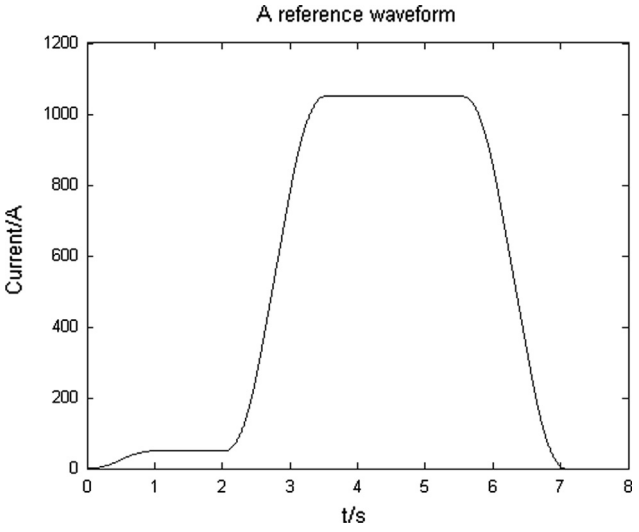

Fig. 1. Typical current waveform of the pulse power supply.

Table 1
Main parameters of prototype & CSR dipole power supply.

Parameters	Digital power supply prototype	CSR dipole power supply
Load Resistance	53.3 mΩ	11.5×17 mΩ
Load Inductance	106 mH	31.4×17 mH
Maximum Output Current	1150 A	2820 A
Maximum Output Voltage	185 V	860 V
Tracking Error (ramp up)	$\leq \pm 1.0 \times 10^{-4}$ f.s.	$\leq \pm 2.0 \times 10^{-4}$ f.s.
Tracking Error (flattop)	$\leq \pm 1.0 \times 10^{-5}$ f.s.	$\leq \pm 1.0 \times 10^{-5}$ f.s.
Ramp up Speed	1150 A/s	934 A/s
Relative Ripple Current	$\leq \pm 2.0 \times 10^{-5}$ f.s.	$\leq \pm 5.0 \times 10^{-5}$ f.s.

2.2. Power circuit

The power supply uses a multi-level converter [6] topology (Fig. 2). It consists of two modules in parallel connection. Each module is composed of two H-bridge converters in series. The series connection topology provides a higher output voltage while the parallel connection topology provides a higher output current. All H-bridge converters work in chopper mode with a switching frequency of 10 kHz; therefore, the frequency in output stage is double as much as the IGBT switching frequency. At the same time, the PWM drive pulse phase is shifted 45° compared with the ones of neighbor converters. As a result, the equivalent frequency in output stage is double again. In this way, ripple current [7] will be inhibited and the response of power supply will be fast enough.

2.3. Control strategy

The aim of the digital control is twofold: make the power supply satisfy the specification (mostly the small tracking error) and make the two modules work in the same way by drawing the same amount of current from both of them [8]. The classic proportion-integral-differential (PID) method is applied. The control system is composed of three feedback loops, shown in Fig. 3. The outer loop is the master loop [9], which regulates the output current. The others are current-sharing loops, which keep the balance of the two modules.

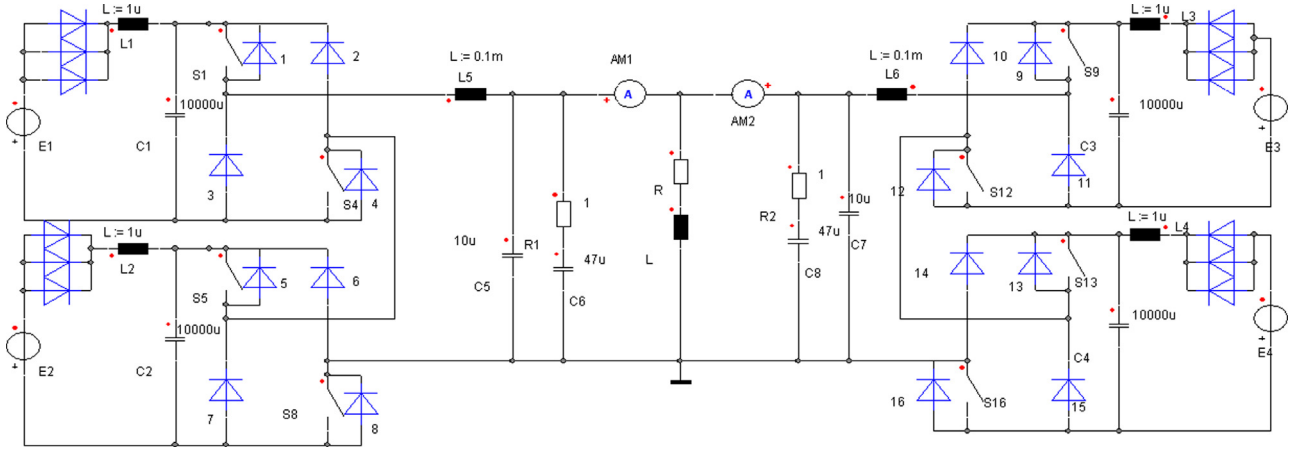

Fig. 2. Topology of the prototype.