Nuclear Instruments and Methods in Physics Research A 725 (2013) 175–178

Contents lists available at SciVerse ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

SCOTT: A time and amplitude digitizer ASIC for PMT signal processing

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Representing the KM3NeT Consortium

ARTICLE INFO

Available online 10 December 2012

Keywords:
Neutrino detection
KM3NeT
PMT
PMT signal processing
Time-over-threshold
ASIC

ABSTRACT

SCOTT is an ASIC designed for the readout electronics of photomultiplier tubes developed for KM3NeT, the cubic-kilometer scale neutrino telescope in Mediterranean Sea. To digitize the PMT signals, the multi-time-over-threshold technique is used with up to 16 adjustable thresholds. Digital outputs of discriminators feed a circular sampling memory and a “first in first out” digital memory. A specific study has shown that five specifically chosen thresholds are suited to reach the required timing accuracy. A dedicated method based on the duration of the signal over a given threshold allows an equivalent timing precision at any charge. To verify that the KM3NeT requirements are fulfilled, this method is applied on PMT signals digitized by SCOTT.

1. Introduction

The KM3NeT consortium [1] is currently preparing for the construction of a cubic-kilometer scale neutrino telescope in the Mediterranean Sea. The charge current interaction of a muon neutrino produces a muon. The Cherenkov light emitted by the muon while crossing the telescope is detected by a three-dimensional array of photomultiplier tubes (PMTs). The time and charge of the PMT signals allow the direction and energy reconstruction of the muon track.

To achieve the required muon angular resolution of 0.1°, it was shown that the PMT pulse from a single photon must be measured with a timing precision better than 2 ns RMS [2] and a charge estimate in the dynamic range up to 100 photoelectrons (pe) [2,3].

A custom analogue-to-digital data processing ASIC was developed based on the time over threshold (TOT) technique to read out the PMT signals. This ASIC, named SCOTT, has to address the high counting rate environmental background signals [4] while keeping good performance on the single photoelectron pulse. A specific method, based on the time over threshold, has been developed to retrieve the pulse time and charge from the ASIC output data. The method has been implemented and fully tested.

The principle of data processing of the SCOTT ASIC with its technical details and performances are described in the following section. Then the algorithm development and data analysis for PMT signal processing are presented. The performances of the ASIC reading a PMT are presented in the last section.

2. The SCOTT ASIC

2.1. Original data processing

The SCOTT ASIC original concept of data processing uses a double sampling strategy. The analogue PMT signal is input in parallel to several channels, sampled first in amplitude in a discriminator and then in time in a digital memory (Fig. 1). The output is a digital waveform of which the amplitude accuracy depends on the number of used channels while the time accuracy is a function of the frequency of the sampling clock.

2.2. ASIC architecture

The SCOTT ASIC is built in AMS BiCmos 0.35 μm process technology. It is a data driven multi-channel circuit including 16 channels with independent inputs (Fig. 2). Each channel is divided into three sub-circuits: one asynchronous stage and two synchronous systems.

The first sub-circuit is an analogue comparator composed of a switch network, a differential discriminator and a 10-bit digital to

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http://dx.doi.org/10.1016/j.nima.2012.11.164

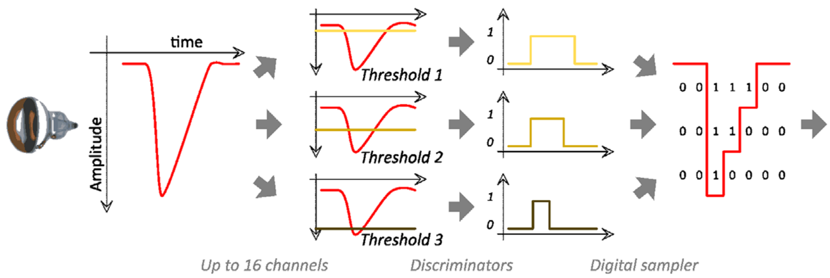

Fig. 1. Principle of SCOTT ASIC data processing. The analogue signal is sampled first in amplitude then in time.

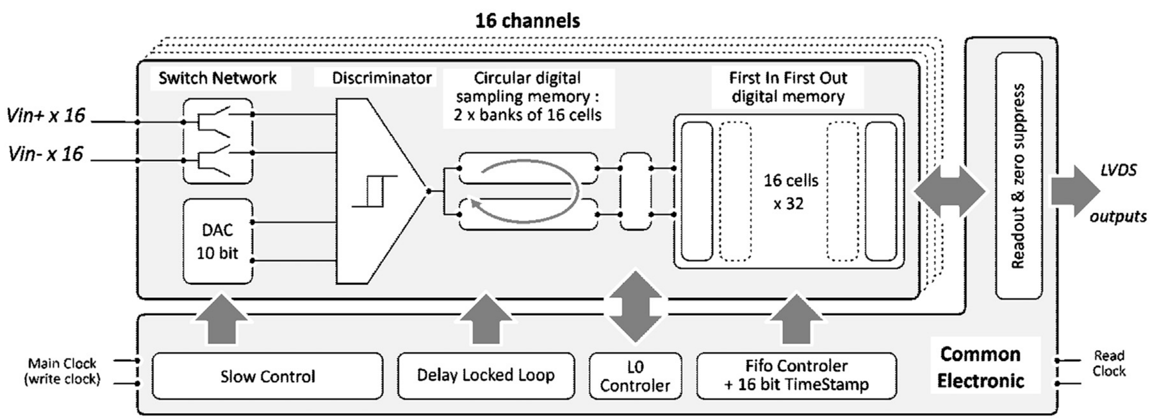

Fig. 2. Top schematic of the SCOTT ASIC.

analogue converter (DAC). The switch network is optionally used to route one analogue input signal up to eight discriminators inside the ASIC. The DACs are differential with a resistor string architecture [5] to guarantee their monotonicity. They can be individually programmed through a slow control interface compatible with the serial to parallel (SPI) protocol. Any of the 16 channels, or a combination of them, can be used as a trigger condition.

In the second sub-circuit, the digital outputs of discriminators are sent to a 32 cell circular digital memory. The sampling frequency is controlled by a delay locked loop (DLL) which produces an equal delay between the 32 clock commands. With a nominal input clock frequency at 50 MHz, the time interval between delayed clock is 20 ns/16 = 1.25 ns. The circular memory is divided into two subsets working alternatively with one subset in writing phase while the second subset is connected to a "first in first out" (FIFO) digital memory. The subsets are divided into 16 cells, or "time slices" of 20 ns. If at least one cell of data matches the trigger condition, all 16 time slices are stored. After one clock cycle, the subsets are inverted and the newly written cells are connected to the FIFO whereas the 16 cells already read out switch to the writing phase. In order to synchronize the data for post-processing reconstruction, a 16-bit time stamp provided by an internal clock counter is added to each time slice.

The FIFO, the third sub-circuit, has a depth of 32 time slices corresponding to a maximum of 640 ns continuous waveform with the nominal clock frequency. It has a double port architecture with a readout clock optionally different from the sampling clock. Data loss can occur due to the limited size of the FIFO and to the Poisson distributed arrival time of the photons. The depth of 32 time slices was chosen to reduce the data loss to approximately 1% for Poisson distributed input rate with a 1 MHz average using three thresholds leveled at the signal amplitude produced by a single photon. During the readout of the FIFO, a zero suppression process is applied. It consists in sending exclusively the channels which have a recorded signal.

Table 1
Main SCOTT ASIC measured parameters.

Circuit	Parameter	Measure
Discriminator	Bandwidth[a]	180 MHz
	Noise	< 0.7 mV RMS
	Offset	< 4.9 mV RMS
	Dynamic range[b]	3 V
DAC	INL	< 0.5 LSB
	DNL	< 0.5 LSB
	LSB	2.85 mV
ASIC	Timing resolution	800 ps RMS
	Power	250 mW

[a] Worst case scenario using the internal switch network.
[b] Differential.

2.3. ASIC performances

The ASIC has been tested in laboratory with a HP 8111A pattern generator and a 10-in. PMT. The performance of the SCOTT ASIC is detailed in Ref. [6]. The main parameters are summarized in Table 1. The expected performances are achieved for most of the measurements. Only, the measured discriminator offset is higher than expected (1 mV RMS). In practice, it can be easily compensated by calibration.

The ASIC SCOTT digitizes PMT signals via amplitude and time sampling. In the case of the 10-in. PMT option [2], the main parameters required for the muon track reconstruction are the pulse time and the pulse charge. In the following section, using a set of PMT pulses digitized with an oscilloscope, two algorithms developed to retrieve the pulse time and charge are described.