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Data readout system utilizing photonic integrated circuit

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ABSTRACT

We describe a novel optical solution for data readout systems. The core of the system is an Indium-Phosphide photonic integrated circuit performing as a front-end readout unit. It functions as an optical serializer in which the serialization of the input signal is provided by means of on-chip optical delay lines. The circuit employs electro-optic phase shifters to build amplitude modulators, power splitters for signal distribution, semiconductor optical amplifiers for signal amplification as well as on-chip reflectors. We present the concept of the system, the design and first characterization results of the devices that were fabricated in a multi-project wafer run.

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1. Introduction

Recent high-energy physics experiments aim to build large-volume detectors. The principle of operation is dependent on the specific application, however all of them tend to generate huge amounts of output data. Generally, the scale of the project requires from the constructors extreme performance of the whole system, from the mechanics, electronics, data transfer and software point of view. A very important part of the detector is the data readout system, which has to be robust and reliable. This task is typically done by means of an optical core network in which the photonic devices (transmitters, modulators, receivers) are driven by electrical circuits [1–4]. The front-end readout is performed by electrical devices. However, none of the systems presented so far makes use of a complex photonic integrated circuit (PIC) in which a high number of optical functions have been combined.

In the coming years photonic ICs are believed to play an increasing role in many fields, especially in telecommunications, but also in datacommunications, medicine, metrology, sensing and others. In comparison to bulk fiber-optic or electrical equivalents, photonic integrated circuits offer advantageous performance in terms of size and weight, energy consumption, operational speed and bit-rate . Furthermore, photonic integration will also help to reduce the packaging cost of the devices as several functionalities (light generation, modulation, multiplexing) will be integrated on a single chip.

There are several technologies in which one can design and fabricate a photonic IC. The most important two are the Indium-Phosphide (InP)-based and Silicon (Si)-based technologies. The big advantage of the latter is that the technology is very mature and offers low-cost and large-scale fabrication of devices. However, due to the fundamental problem of the indirect bandgap of Silicon, efficient light generation is not possible, and Si-based circuits are limited to using passive components, modulators and detectors. On the other hand, InP-based materials, such as the quaternary alloy InGaAsP have a direct bandgap and are used for light generation and detection in the 900–1650 nm window. This enables the monolithic integration of passive components (waveguides, splitters, filters) with amplifiers, detectors and phase modulators. With these components, more complex circuits containing laser light sources, receivers, switches and routers can be fabricated.

InP-based photonics technology is increasingly mature and nowadays chips consisting of hundreds of components have been fabricated [5]. In addition, a radically new way to fabricate photonic ICs is being explored. Instead of developing a new technology almost for each new component or circuit, this new fabrication technology is standardizing on a few basic building blocks from which larger components and complex circuits can be synthesized. This new concept is being developed within the framework of European FP7 Projects EuroPIC [6] and PARADIGM [6]. The generic integration technology is based on the ideas taken from the silicon microelectronics approach. CMOS technology makes use of transistors, resistors and capacitors to build circuits that can be used for a very wide variety of applications. In InP photonics these basic building blocks can be a waveguide, a phase modulator, a semiconductor optical amplifier (SOA) and a polarization converter. More complicated components, such as power couplers and splitters, (de)multiplexers, on-chip reflectors, amplitude modulators, space-switches, various types of laser light sources, detectors and polarization

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independent devices may be built using such building blocks. As a result, even highly complex circuits dedicated for different application fields may be designed and fabricated in a single technology process. We believe that once the generic model is established and fixed, it will reduce the cost of fabrication of a single chip by more than an order of magnitude. It will enable the access to cutting edge technology for small and medium enterprises as they will be able to apply photonic ICs in their devices and systems without the necessity of large investments in cleanroom facilities or technology development.

Another important idea which origins from the silicon microelectronics is the concept of a multi-project wafer (MPW) run. This helps to reduce the cost of fabrication of photonic ICs as the area of the wafer is divided among many users, who pay for the chips proportionally to the occupied space. The MPW concept helps in reduction of research and development costs, as it enables low-cost prototyping. However, as such a run should be application blind, there has to be a fixed technology process in which the users design their circuits. Additionally, there have to be strict design-rule checks as the designs should not affect the neighboring cells. At present, the application of the concept of MPW runs in InP in photonics is being investigated. The COBRA Research Institute in Eindhoven (The Netherlands) already offers a small-scale access to MPW runs [6] and first trials have been performed at Oclaro in Caswell (UK) and Heinrich-Hertz Institut in Berlin (Germany). All involved parties are members of JePPIX, the Joint European Platform for InP-based Photonic Integrated Components and Circuits [6–8].

In this paper we present the concept of a readout system architecture, implemented in an InP-based photonic IC. This application specific photonic integrated circuit (ASPIC) is dedicated for use in a large-volume detector. We also present the first characterization results of the ASPICs that were designed in a generic approach and fabricated in MPW runs at Oclaro, within the framework of EuroPIC and the Dutch smartmix project Memphis [8].

2. EuroPIC Project

The European FP7 Project EuroPIC (European Manufacturing Platform for Photonic Integrated Circuits, europic.jeppix.eu) started in August 2009. It is a collaboration of key players in the European InP photonics—chip and packaging foundries, software companies, R&D companies, universities and also application users of the photonic devices.

The main objective of the project is to establish a standard production chain based on the generic technology approach. The concept of such a chain is shown in Fig. 1. When a user has a concept of an application for a photonic IC, he can do the design by himself or ask a design house to do it for him. Once the design is complete, the resulting mask layout is sent to the foundry where the chip is fabricated. If the user wants to have the ASPIC packaged, the fabricated chips are sent to the packaging foundry. Eventually, the user receives the packaged devices for characterization and testing.

To establish such a chain, several objectives have to be reached. First of all, the foundry has to determine and describe the properties and the performance of the available building blocks in a design manual. Secondly, for an effective design process, there has to exist some dedicated software which has to enable simulations of basic and complex components, and eventually even full circuits. Additionally, it has to provide the possibility of making a mask layout and implement automated checks for violation of the foundry design rules. Furthermore, a standard for packaging has to be developed. This includes

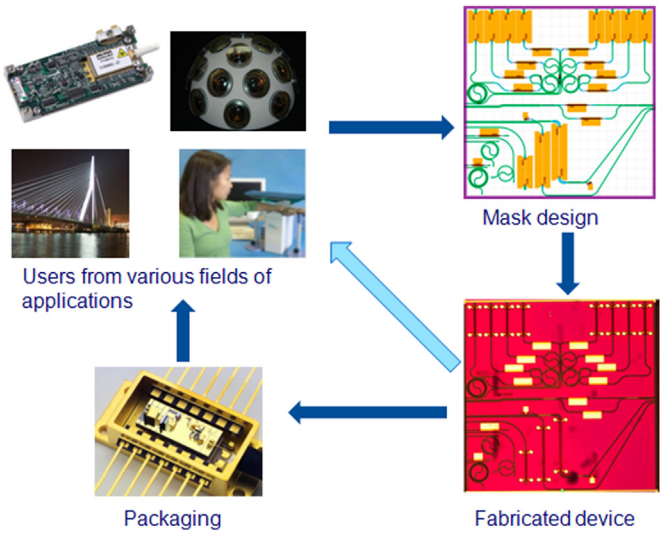

Fig. 1. Concept of the generic technology production chain.

specification of the chip dimensions and of the number and the position of the optical and electrical interfaces to and from the chip. Finally, the foundry has to elaborate the validation process of the fabricated devices. The partners of EuroPIC are currently working to reach these objectives and the first results are very promising [9,10].

Additionally, EuroPIC aims to prove that chips fabricated in the very same technology process can be successfully used in various fields of application, such as telecommunications (access networks, Radio-over-Fiber systems), medicine, data read-out and sensing. On an early run, ten ASPICs were simultaneously designed and the mask layouts have been combined in a MPW run. This was the first of two planned runs at Oclaro and Heinrich-Hertz Institut each, and the chips are now being characterized. The second run is currently under way. Two of the fabricated ASPICs will be used to test a generic packaging scheme, developed by CIP Photonics (Ipswich, UK).

3. System architecture and the serializer concept

One of the EuroPIC pilot applications is the front-end readout unit for a neutrino telescope. Although for this application the specifications have been taken from the KM3NeT project [11], the proposed solution is sufficiently general to make it suitable for use in other experiments.

KM3NeT aims at development and deployment of a cubic kilometer size neutrino telescope. The idea is to place hundreds of thousands of photomultipliers at the bottom of the Mediterranean Sea. They will be housed in optical modules (glass spheres), 31 photomultipliers in each. The output data from the photomultipliers has to be read out with a frequency of 333 MHz, the transmission bit-error rate (BER) should be kept below 10^{-9} and the power consumption inside a single module should not exceed 7 W. The concept of the readout system proposed for the KM3NeT detector by NIKHEF, the Dutch National Institute for Subatomic Physics, makes use of continuous wave lasers and receivers in the shore station, a fiber link with inline erbium-doped fiber amplifiers between the station and optical modules, a reflective electro-absorption modulator and an electrical serializer inside an optical module [4]. The modification we propose is to replace the electrical serializer with a photonic integrated circuit, simultaneously increasing the sampling frequency up to 1 GHz and keeping the BER coefficient unchanged.

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